PE42525 and PE426525 Performance Optimization

Application Note 66

Summary

This application note provides the recommended landing pattern and assembly process for achieving optimum performance with the PE42525 and PE426525. The PE42525 and PE426525 are flip-chip, single-pole double-throw (SPDT) switches that support a wide frequency range from 9 kHz to 60 GHz. The PE42525 is suited for test and measurement (T&M), microwave backhaul and radar applications. The PE426525 is ideal for applications that require extended temperature support in the
–55 °C to +125 °C range, such as harsh industrial applications.

Introduction

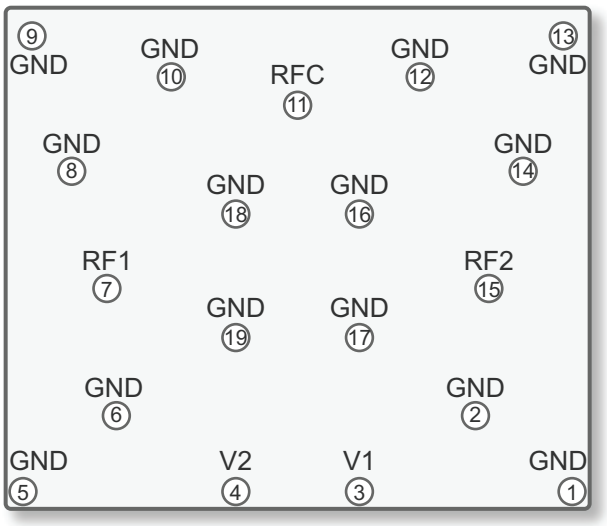
PE42525 and PE426525 are the first 60 GHz millimeter-wave switches to harness the high-frequency performance of UltraCMOS®. Monolithic microwave integrated circuit (MMIC) design techniques are used to achieve unprecedented performance in the K and Ka microwave and millimeter-wave bands. Achieving 1.9 dB of insertion loss and greater than 37 dB of isolation at 50 GHz, the PE42525 and PE426525 reflective SPDT switches deliver the same high-power, high-linearity performance for which pSemi's UltraCMOS technology is historically known.

Product Overview

The PE42525 and PE426525 are flip-chip SPDT switches that use lead-free solder ball technology to provide the signal and ground interconnect. Solder reflow profiles common to lead-free surface-mount device (SMD) assembly can be readily used to achieve uniform and reliable attachment.

Figure 1 shows the pin configuration for the PE42525 and PE426525. **Table 1** provides detailed pin descriptions. To ease routing and manufacturing, the pin configuration maintains a minimum of 500 µm (0.5 mm) pitch between all unique signal pads.

Figure 1 ▪ Pin Configuration (Bumps Up)[*)]



Note: * Drawing is not drawn to scale.

Table 1 ▪ Pin Descriptions

Pin #	Pin Name	Description
1, 2, 5, 6, 8–10, 12–14, 16–19	GND	Ground
3	V1	Control input 1
4	V2	Control input 2
7	RF1	RF port 1
11	RFC	RF common port
15	RF2	RF port 2

Landing Patterns

The PE42525 and PE426525 are configured with a 0.5 mm, or 500 µm, minimum ball pitch. Thin film technologies can readily meet the line width and spacing critical dimensions (CDs) of 100 µm or less. Other thick film and PCB processes, by comparison, generally require significantly less stringent CDs to achieve reasonable and consistent manufacturing yields. The comparatively wide 500 µm ball pitch supports large CD requirements and allows the die to be assembled directly to RF PCBs.

For optimum microwave performance, specific metallization and via patterns are defined and implemented to provide measured results for the PE42525 and PE426525. These recommended layouts can be downloaded from the pSemi website at http://www.psemi.com.

Alumina Substrate

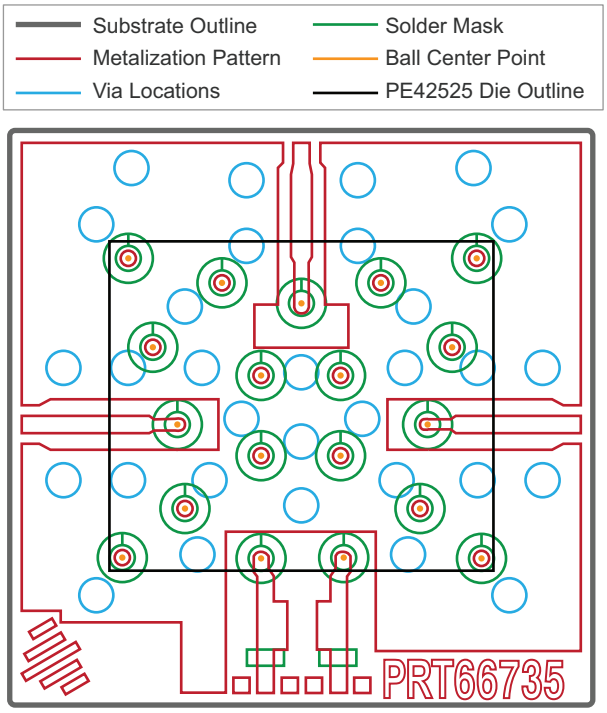
Figure 2 and **Figure 3** show two recommended metalization patterns and via placements for alumina substrate carriers on which the PE42525 and PE426525 are assembled. The first substrate carrier uses an alumina thickness of 10 mil with 8 mil diameter vias (see **Figure 2**). Important parameters for the coplanar waveguide with ground (CPWG) transmission lines are:

- RF common port (RFC) transitions from a 50Ω input to a 65Ω line of length and width 12.5 mil and 2.8 mil, respectively.
- RF1 and RF2 ports transition from 50Ω transmission lines (width and spacing of 5.13 mil and 3.54 mil) to 64Ω lines of length and width of 8 mil and 3.2 mil, respectively.

This substrate carrier is referenced as PRT66735. When this substrate is epoxied to a GND plane, the top GND is epoxied to the bottom GND for improving the RF probe to substrate transition for >40 GHz performance, as was performed for characterization. A second substrate carrier using 10 mil alumina with improved RF probe to substrate transitions is the recommended metalization pattern. The PRT67978, shown in **Figure 3**, has additional vias near the RF port edges, along with edge-wrapped features (where top GND metalization is wrap-connected to the bottom substrate metalization) to retain high-frequency performance >40 GHz.

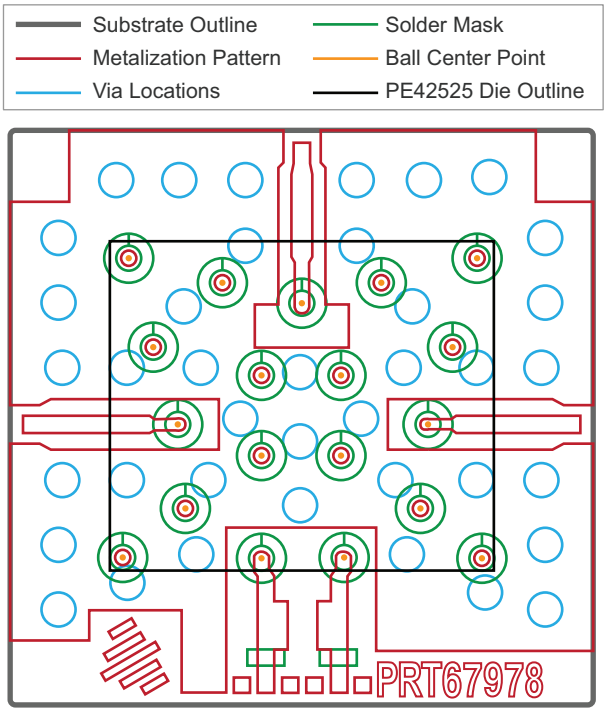
If the end application requires a different thickness alumina between 5–10 mil, the critical dimensions of line width, spacing, and via diameter can be readily scaled to accommodate specific thickness requirements.

Figure 2 ▪ PRT66735 10 mil Alumina Substrate Metalization and Via Pattern(*)



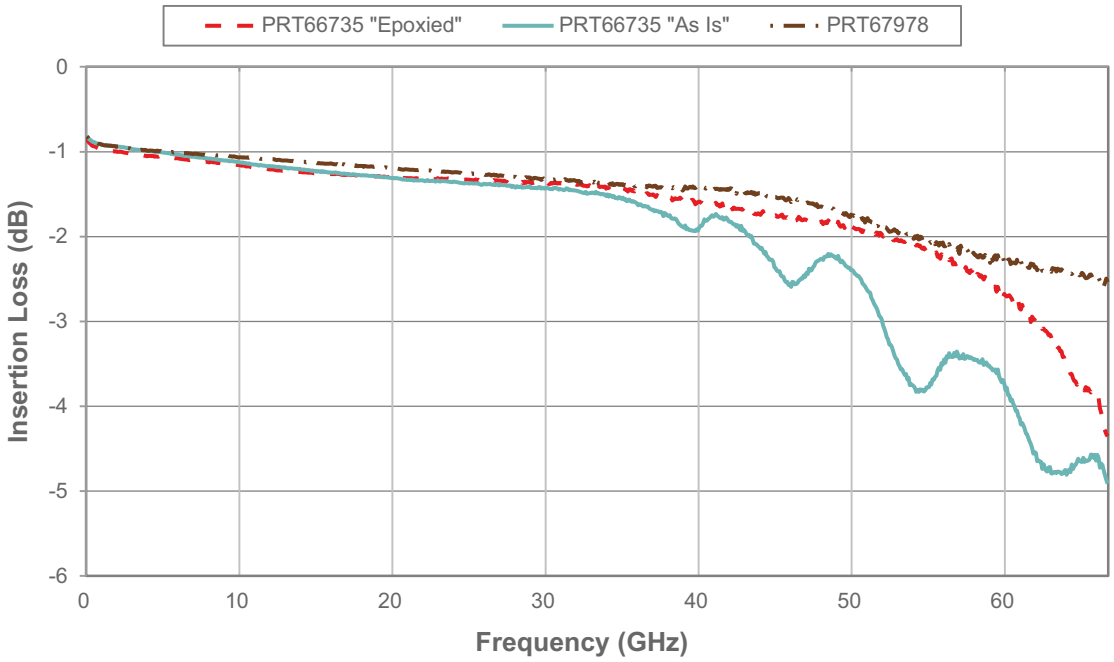
Note: * Used for characterization and sample units.

Figure 3 ▪ PRT67978 10 mil Alumina Substrate Metalization and Via Pattern (recommended)



RF performance can be affected by metalization and via patterns. **Figure 4**, for example, shows changes in insertion loss levels due to grounding differences near the RF probe transitions for the PRT66735. For comparison, the substrate PRT67978 used for present sampling of the PE42525 and PE426525 is also shown. The epoxied PRT66735 substrate and edge-wrapped PRT67978 substrate eliminate insertion ripple for frequencies over 40 GHz.

Figure 4 ▪ Insertion Loss Performance Comparison(*)

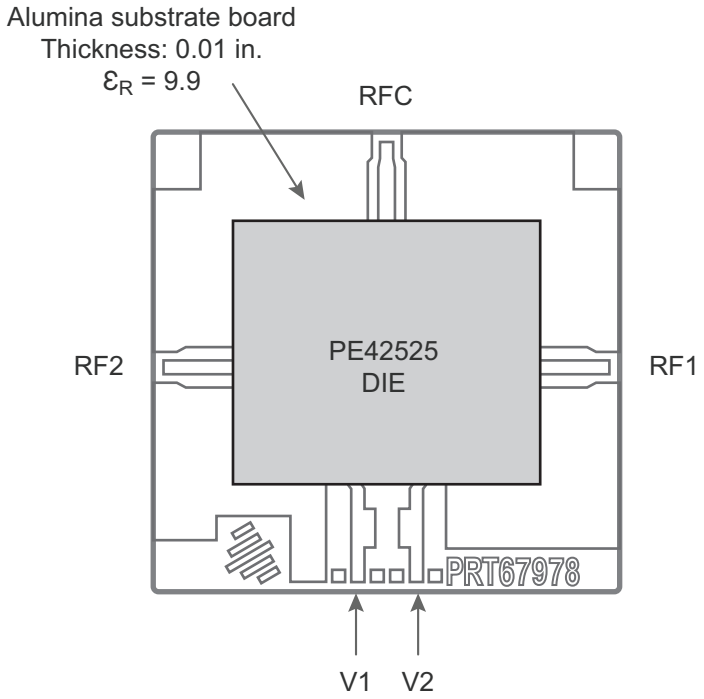


Note: * Comparison is between 10 mil alumina substrate carriers PRT66735 (with and without epoxy) and PRT67978 metallization and via patterns. PRT67978 is the recommended pattern. PRT66735 with epoxy grounding was used for characterization.

Figure 5 ▪ Modified PRT66735

Note: * Epoxy was used to connect top metal GND to bottom GND plane for improved RF probe to substrate transition.

Figure 6 ▪ Assembled PE42525 on Alumina Substrate PRT67978



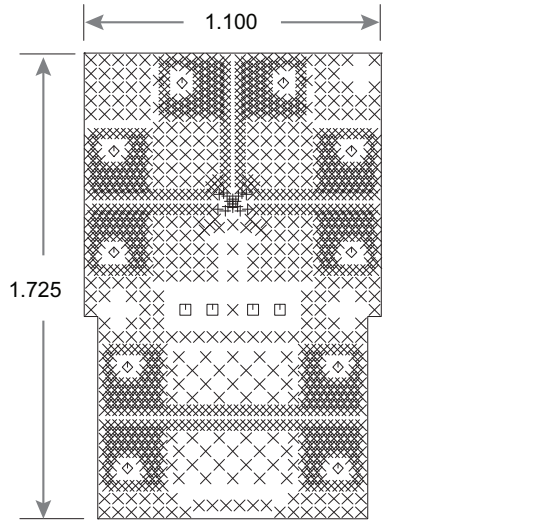
To minimize unwanted wicking of individual solder balls from the local connection point, use a solder stop such as a marking, protective polymer layer, or other material recommended by the substrate manufacturer. The solder stop thickness should be 15–25 µm to prevent the solder wicking from touching the face of the PE42525 die.

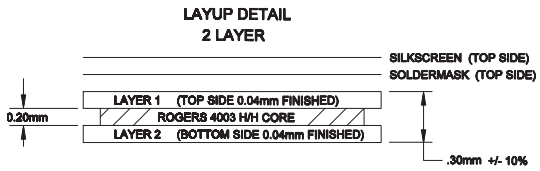
To facilitate accurate measurements, the line width and spacing at the edge of the RF lines in the landing pattern are configured for 150 µm pitch ground-signal-ground (GSG). Users can modify and integrate the landing pattern anywhere outside the die outline to align with the higher level assembly and substrate design requirements.

Rogers 4003 Printed Circuit Board

Metalization and via pattern PRT61038 have been generated for a Rogers 4003 substrate. **Figure 7** shows the pattern for an 8 mil board thickness. Although this board layout is configured for high-frequency SMA connectors, the basic pattern can be used to create an RF-probable PCB (see **Figure 8**). The measured performance of a PE42525 that is assembled to the RF probe-able PCB and properly de-embedded performs comparably to an alumina-based design.

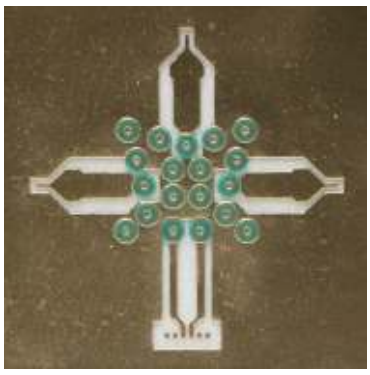
Figure 7 ▪ PCB Rogers 4003 PRT61038 Metalization and Via Patterns





SIZE	QTY	SYM	PLATED	TOL
0.006	17	+	YES	+.000/−0.005
0.008	1139	X	YES	+.000/−0.008
0.037	4	□	YES	+/−0.003
0.081	10	◇	YES	+/−0.003

Figure 8 ▪ PCB Rogers 4003 Evaluation Board (*)



Note: * Based on PRT61038 metalization and via patterns.

In addition to the 50Ω transmission line width and spacing, the dimensions of the thinner lines right at the PE42525 SPDT RF ports must also be considered. The RFC port transitions from a 50Ω line to a line length and width of 21 mil and 6 mil (Z = 75Ω), respectively. The two RF ports, RF1 and RF2, transition from a 50Ω line to a line length and width of 16.5 mil and 6 mil (Z = 75Ω), respectively. These parameters serve as alternate matching impedances that can yield similar results if the transmission line impedances used for the alumina substrate are used for the PCB. Via diameters are 8 mil, except for the region under the die, which uses 5 mil diameter.

Assembly Process

Assembling the PE42525 and PE426525 leverages common SMD solder reflow techniques. **Figure 9** shows a reflow profile suitable for use with an alumina substrate and which follows a recognized JEDEC profile. Observe the following recommendations when attaching the PE42525 and PE426525:

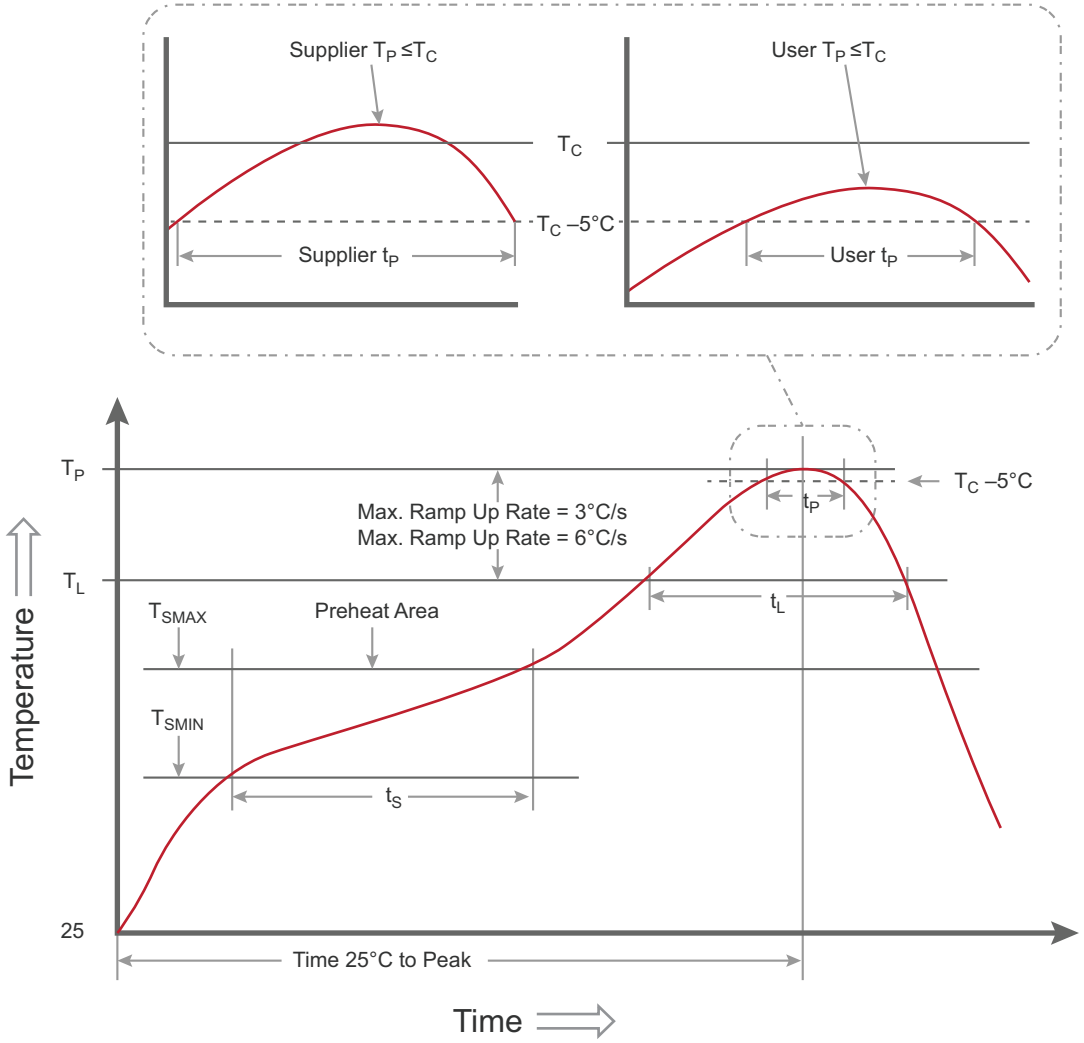
- No solder paste needs to be printed.
- Apply a thin layer of flux by stencil printing.
- Pick and place the die, and align it on the substrate.
- Conduct reflow using a controlled reflow profile (refer to JSTD020D-01).
  - Lead-based reflow: *Table 4-1*
  - Lead-free reflow: *Table 4-2*
  - Reflow definition: *Section 5.6* and *Figure 5-1*
- Check for alignment and voids in joint using x-ray inspection after reflow.

Observe these assembly guidelines when attaching the PE42525 and PE426525 to an alumina-based substrate. If a PCB is used, pay attention to the substrate material, its glassivation temperature, and the material coefficient of thermal expansion (CTE) when defining a reliable reflow profile. Excessive soak times or temperatures can cause significant assembly yield issues.

There is an important distinction between a PCB configured with a high-frequency connector and RF probe-able alumina boards. Measured results of PCBs with connectors exhibit high-frequency RF performance limitations related to the limitations of the RF connector to board transitions.

Improved RF performance of PCBs configured with connectors is achieved by using a core-only PCB as in PRT61038 (8 mil board) instead of PCBs with a core plus laminate buildup, which results in a 62 mil thick board. An RF-probed substrate board delivers the true RF performance of the die.

Figure 9 ▪ Generalized Reflow Profile (*)



Note: * Reference JEDECJ-STD-020D.1 *Figure 5-1* and *Figure 5-2*.

Recommendations for Attaching the PE42525 and PE426525 on a PCB

When defining a reliable reflow profile, pay attention to the PCB substrate material, its glassivation temperature, and the various CTEs. Excessive soak times or temperatures can cause significant assembly yield issues and potentially laminate delamination.

Table 2 through **Table 4** list assembly-related process parameters that can help define an assembly flow for specific high-frequency PCB substrates. When refining a suitable reflow profile and assembly process, also consider other components on the same PCB, the PCB substrate temperature limitations, and the PCB board design and its thermal properties.

Table 2 ▪ PE42525 and PE426525 Assembly-Related Parameters

Parameter	PE42525 and PE426525	Unit	Comments
Max reflow temperature, T_P	≥260	°C	JEDEC J-STD-020D.1 *Table 4-2*
Max dwell at T_P	10	sec	JEDEC J-STD-020D.1 *Table 5-2*
Recommended flux			
Pb-free solder ball	Tin-95.5/Ag-3.5/ Cu-1 (%)		SAC 351 solder definition
Min landing size	90	µm	
Solder stop max thickness	25	µm	
Solder stop diameter max	120	µm	
Solder paste particle size	Type 5		If deemed necessary, 15–25 µm particle size
Stencil thickness	60	µm	
Stencil aperture diameter	180	µm	
CTE (worst case X, Y, Z)	6–7	ppm/°C	
Underfill	Not recommended		If deemed necessary, a low loss, low dielectric constant underfill is recommended.

Table 3 ▪ Assembly Related Parameters for Common High-Frequency PCB Substrates

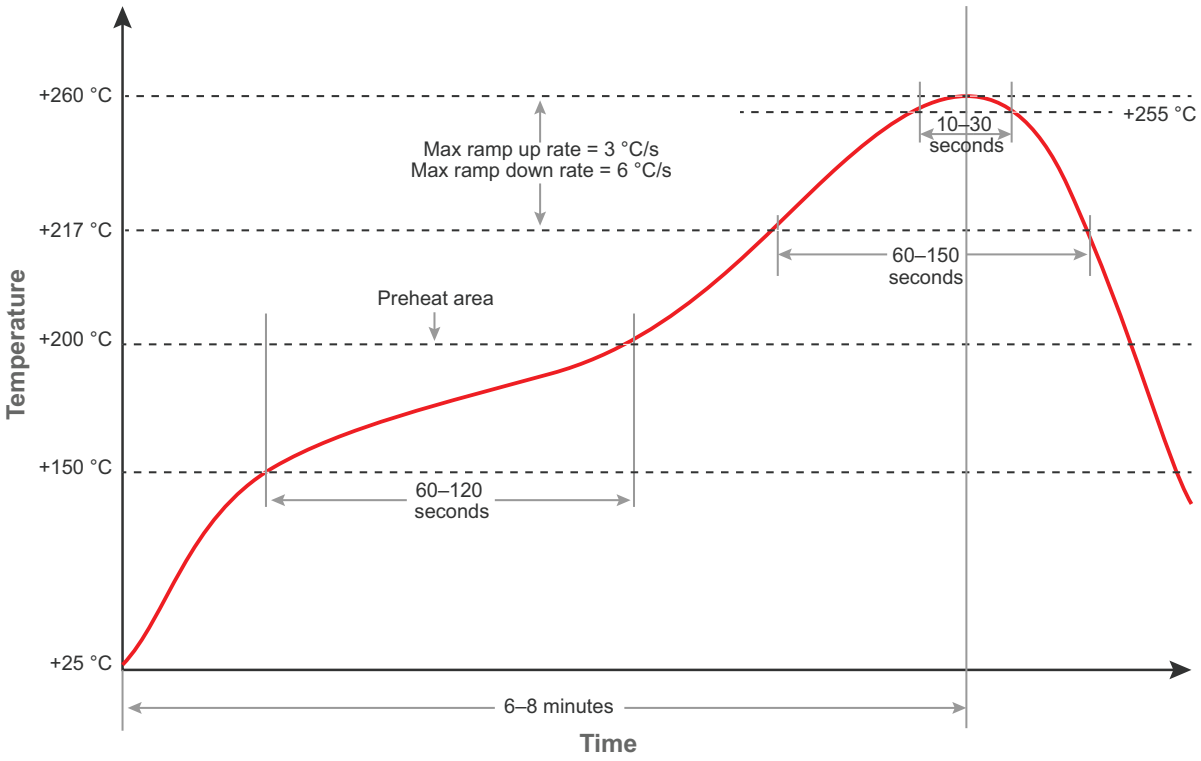
Parameter		Panasonic Megtron 6	Rogers 4350	Rogers 4003	Unit
Max reflow temperature, T_P		≥260	≥260	≥260	°C
Max dwell at T_P		10	10	10	sec
Glassivation temperature, T_G		180–210	>280	>280	°C
CTE (worst case X, Y, Z)	X		10	11	ppm/°C
	Y		12	14	
	Z	45	32	46	

Table 4 ▪ Reflow Profile Parameter Recommendations(*)

Parameter	Pb-free Assembly	Unit	Comments
Preheat temperature	150–200	°C	
Preheat time	60–120	sec	
Ramp up rate	3	°C/sec	
Liquidous temperature, T_L	217	°C	SAC 351 melting point
Time above T_L	60–150	sec	
Peak temperature, T_P	260	°C	
Time within 5 °C of T_P	10–30	sec	
Time 25 °C to T_P	6–8	min	
Ramp down rate	3–6	°C/sec	

Note: * Source is JEDEC J-STD-020E.

Figure 10 ▪ Suggested Starting Definition for PCB Reflow Profile



Measured Performance Beyond 60 GHz

Figure 11 shows the insertion loss behavior up to 67 GHz of the PE42525 and PE426525 when mounted to the PRT67978 alumina substrate carrier and measured in an RF probe configuration. **Figure 12** shows 14 dB return loss and 38 dB isolation performance out to 67 GHz.

Figure 11 ▪ Insertion Loss on 10 mil Alumina Substrate Carrier

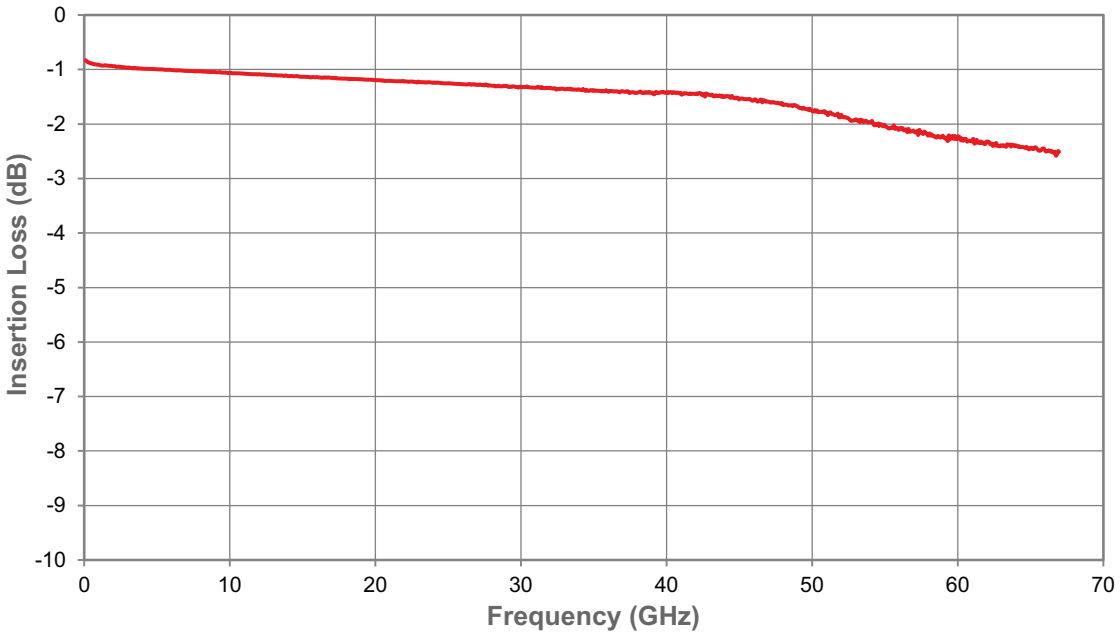
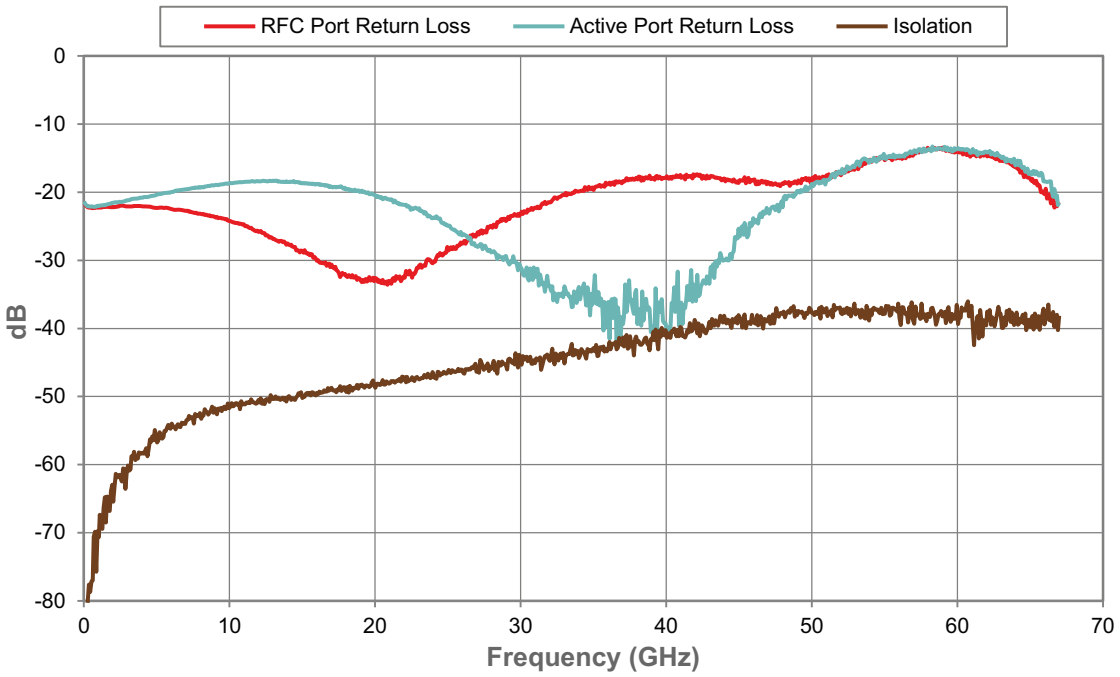
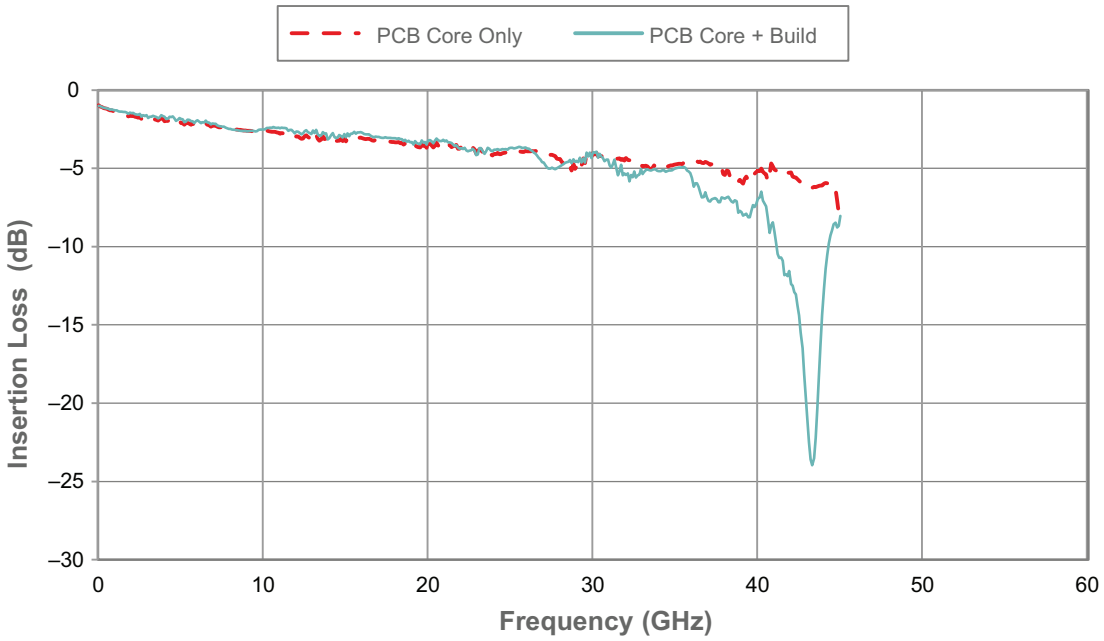


Figure 12 ▪ Return Loss and Isolation on 10 mil Alumina Substrate Carrier



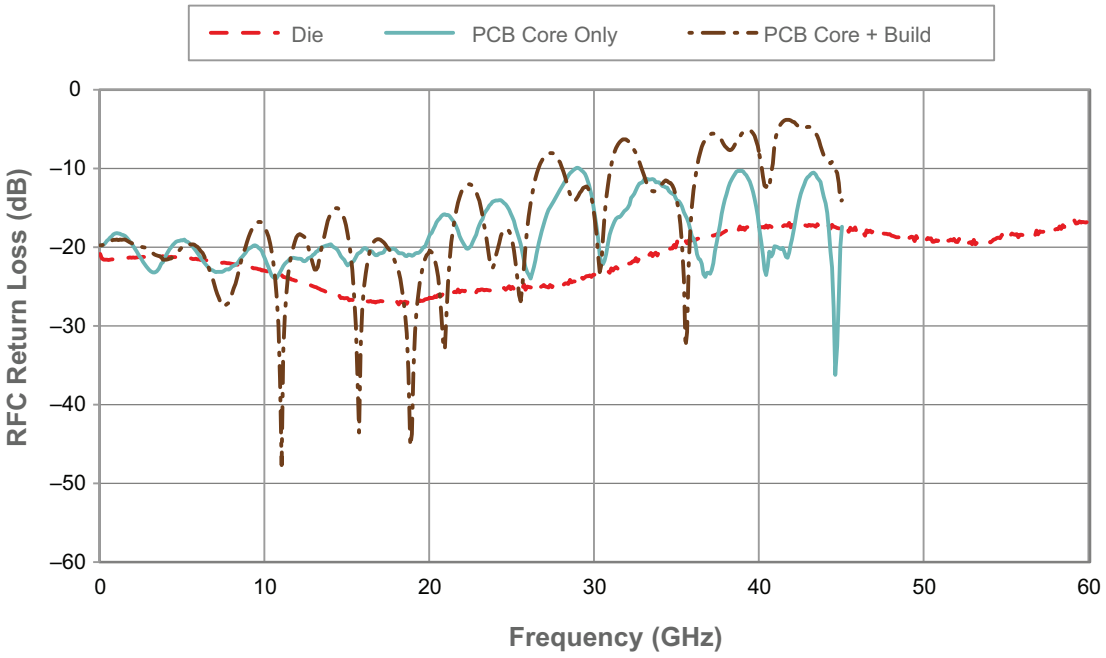
Similarly, for Rogers 4003 substrates, **Figure 13** shows the insertion loss response to 45 GHz for a "core-only" board (see **Figure 7**) and a "core + build" board that includes a second 370HR laminate-stiffening layer under the core layer. **Figure 14** compares RFC port return losses to die mounted on Rogers 4003 boards configured with connectors versus a die mounted on an RF probed alumina substrate.

Figure 13 ▪ Insertion Loss on 8 mil Rogers 4003(*)



Note: * PCB core only: PRT61038 substrate carrier with RF connectors; PCB core + build: 8 mil Rogers 4003 plus 370HR laminate (62 mil total) with RF connectors.

Figure 14 ▪ Return Loss on Rogers 4003(*)



Note: * Die: RF probe on PRT67978 alumina carrier; PCB core only: PRT61038 substrate carrier with RF connectors; PCB core + build: 8 mil Rogers 4003 plus 370HR laminate (62 mil total) with RF connectors.

Conclusion

PE42525 and PE426525 are the newest millimeter wave switches from pSemi. Both switches deliver competitive insertion loss, exceptional isolation, and high linearity and power handling, along with the uniformity and availability that UltraCMOS affords. To achieve high performance at these frequencies, however, extreme care must be taken to eliminate stray parasitics affecting the RF channel.

The guidelines and best practices in this application note enable users to obtain optimum performance from the PE42525 and PE426525. It includes descriptions of landing patterns in different substrate technologies, which show comparable performance up to 60 GHz. Complete CAD files of the physical layouts are available from pSemi's website to help integrate the PE42525 and PE426525 into higher-level assemblies and systems.

Sales Contact

For additional information, contact Sales at sales@psemi.com.

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