Replacing PE4304 with PE4314

Application Note 63

Objective

The Peregrine PE4314 is the updated digital step attenuator (DSA) designed as a direct replacement for the PE4304 DSA. Although primarily designed as a PE4304 replacement, it can also be used to replace the PE4307, PE4308 and PE43404 devices.

Introduction

The PE4314 is a 75Ω HaRP™ technology-enhanced, 6-bit DSA that supports a frequency range from 1 MHz to 2.5 GHz. It features glitch-less attenuation state transitions and supports 1.8V control voltage and an extended operating temperature range up to +105 °C, making this device ideal for multiple wired broadband applications.

PE4314 covers a 31.5 dB attenuation range in a 0.5 dB step. It is capable of maintaining 0.5 dB monotonicity through 2.5 GHz. In addition, no external blocking capacitors are required if 0 VDC is present on the RF ports.

PE4314 is a pin-compatible upgraded version of PE4304, PE4307, PE4308 and PE43404. An integrated digital control interface supports both Serial and Parallel programming of the attenuation, including the capability to program an initial attenuation state at power up.

Although it was designed to be pin-for-pin compatible with PE4304 there are some subtle differences that should be checked when using PE4314 as a direct replacement.

PE4314 Functional Differences

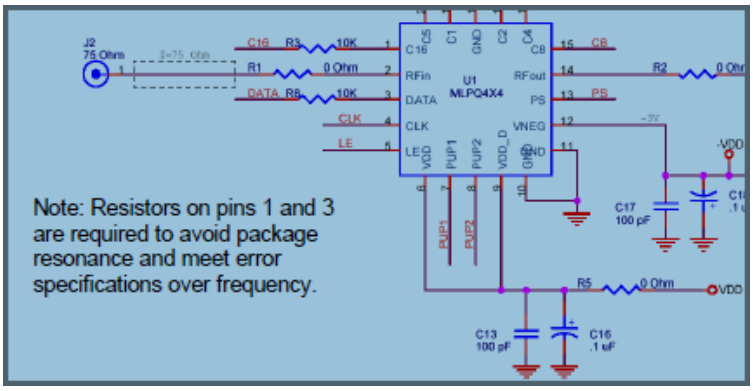
The PE4314 functional differences are specified as:

- The application circuit
- Logic threshold levels

The Application Circuit

The PE4304 application circuit contained two resistors in the C16 and DATA lines.

Figure 1 • *PE4304 Application Circuit*



These resistors were originally placed to remove a resonance between the RF_{IN} pin and the connection to the adjacent pins. This resonance caused degradation in the PE4304 DSA performance at higher frequencies. The PE4314 does not have this degradation. For the PE4314 it is preferable to remove the resistors or reduce the values such that the PE4314 logic threshold levels are met.

Logic Threshold Levels

The PE4304 was designed for 3V logic levels. The logic levels are dependent on the V_{DD} used.

Table 1 • *PE4304 Logic Levels*

Parameter	Min	Typ	Max	Unit
Digital input high	0.7 × V_{DD}			V
Digital input low			0.3 × V_{DD}	V

The PE4314 logic threshold is not dependent on the V_{DD} level. The PE4314 is designed to accept 1.8V logic threshold levels, which have been extended to accept 3.6V logic V_{IH} max.

Table 2 • *PE4314 Logic Levels*

Parameter	Min	Typ	Max	Unit
Digital input high	1.17		3.6	V
Digital input low	–0.3		0.6	V

Users should ensure that the PE4314 logic levels are compatible with the data levels in the design. If the series 10k resistor is left in the circuit on the DATA line or if the clock period is too short, the data V_{IL} threshold may not be met in the high to low transition.

Transferring a PE4304 Design

If the PE4304 design is to be transferred to a new design using the PE4314, it is important to note that the V_{DD} can be increased to 5V. This may allow the removal of a 3V supply and regulator. However, if the higher V_{DD} is used then it is important to note the maximum digital voltage for the PE4314 is still 3.6V. This applies to V_{DD_D}, the SPI logic and static logic pins, such as PUP1/PUP2 and P/S that may be permanently tied to a logic high. These lines must NOT be tied to a 5V V_{DD} line.

Conclusion

The PE4314 can successfully be used to replace the PE4304 in an existing design with appropriate consideration for the logic levels and removal or reduction in value of the DATA line resistors. The PE4314 can also be used in a new design based upon an older PE4304 design provided the maximum digital input voltage remains 3.3V.

Note: The PE4314 transition time and transient amplitude have been greatly reduced from the PE4304 to minimize any signal disturbance during state changes. This is to enable use in higher modulation standard such as DOCSIS 3.1.

Sales Contact

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