Thermal Characterization

Application Note 57

Summary

Thermally driven degradation is one of the primary causes of failure in integrated circuits (ICs). Progressively smaller scaling of CMOS structures has a direct impact on electro-migration and other thermally activated failure mechanisms. Management of the thermal exposure of ICs is critical. The power demands on RFICs can result in high junction temperatures sustained for relatively long periods of time. In addition to the self-heating experienced by power dissipation on the die active area, the ambient temperature of the operating environment has a contributing effect on the overall thermal exposure to the die. A clear and accurate understanding of the thermal handling capability of an IC is critical for proper design and functioning of electronic assemblies.

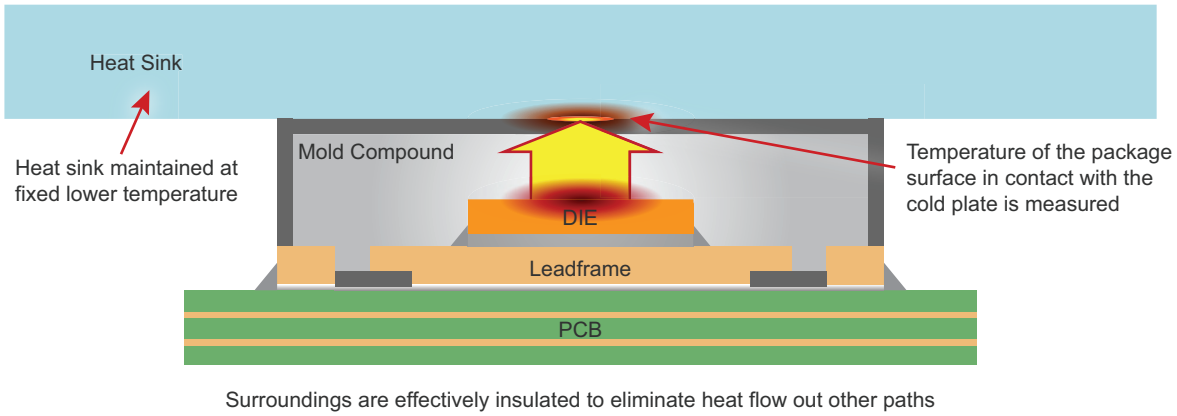
Industry Standards for Thermal Characterization Testing and Reporting

JEDEC committee JC-15 was formed to establish industry standard methodology for thermal characterization techniques for semiconductor packages. JEDEC specification JESD-15 *Thermal Modeling Overview* provides the starting point for characterizing and reporting package thermal characteristics. JEDEC 51-1 identifies the theoretical basis for the testing of single semiconductor devices such as Peregrine's RFICs. Additional JEDEC 15- and 51- series documents provide further details on testing and reporting results.

Some confusion has arisen over the years between the use of theta (Θ) and psi (Ψ) terminology. Thermal characterization parameters (Ψ) are not thermal resistances (Θ). Often, Θ_{JC} is requested when the customer really wants Ψ_{JT}.

Package thermal resistance values (e.g. Θ_{JC}, Θ_{JB}) are established by ensuring that 100% of the heat flow path through the package is captured. This is accomplished by measuring the component power dissipation flowing through either the top or bottom of the package (see **Figure 1**). While the values may be useful for comparing packages, the test conditions don't generally match the user's application. Θ_{JC} was originally defined for components requiring an external heat sink.

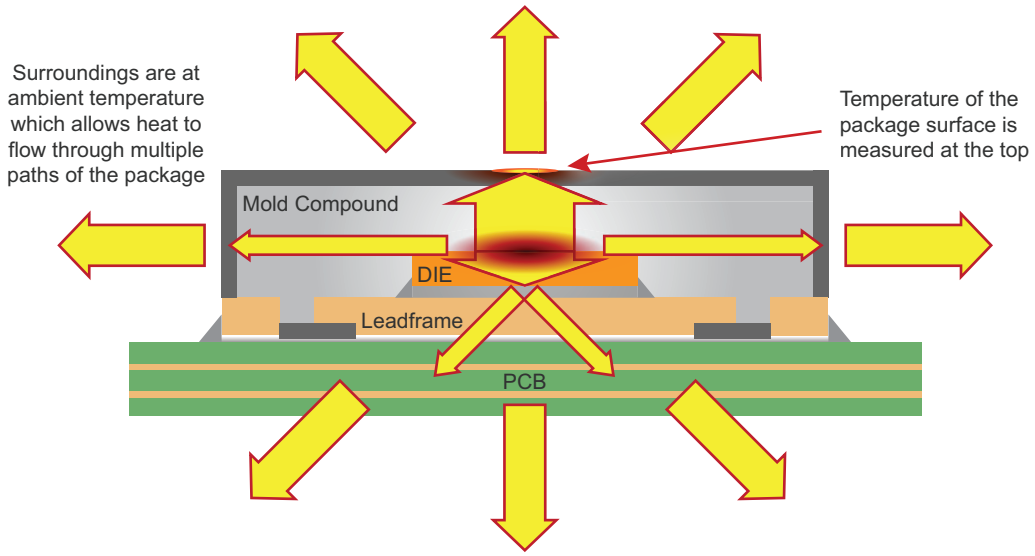
Figure 1 ▪ Example of Θ_{JC} Measurement(*)



Note: * Cross-sectional representation of device mounted to printed circuit board (pink arrows represent heat flow).

When the Ψ parameter is measured, the component power is flowing out of the component through multiple paths which more closely matches the customer application environment. Ψ_{JB} is lower than or approximately equal to Θ_{JB}. Ψ_{JT} is often significantly lower than Θ_{JT} (see **Figure 2**).

Figure 2 ▪ Example of Ψ_{JT} Measurement(*)



Note: * Cross-sectional representation of device mounted to printed circuit board (pink arrows represent heat flow).

Ψ_{JT} is the junction-to-top thermal characterization parameter where T_{TOP} is the temperature at the top center of the package.

$$\Psi_{JT} = (T_J - T_{TOP})/P$$

Ψ_{JB} is the junction-to-board thermal characterization parameter where T_{BOARD} is the temperature measured on or near the component lead.

$$\Psi_{JB} = (T_J - T_{BOARD})/P$$

P is the total power (heat) dissipated in the chip. The power may leave the chip through any thermal path, not just the board.

Users can apply the Ψ equations to estimate the component junction temperature in their application by measuring the external component temperature in the application environment and using the appropriate Ψ thermal characterization parameter. This estimated junction temperature can then be compared with a junction temperature specification to determine if the device is being operated below the maximum operating temperature specification. A component power dissipation estimate is required. Component power dissipation can be estimated by subtracting the insertion loss (in dB; specified in the datasheet) from the input power to the device (in dBm) to derive an output power (in dBm). Conversion of the input power and resulting output power into watts allows a straightforward subtraction to yield the power dissipation (P_{DISS}) of the device. Junction temperature (T_J) can then be calculated using the formula

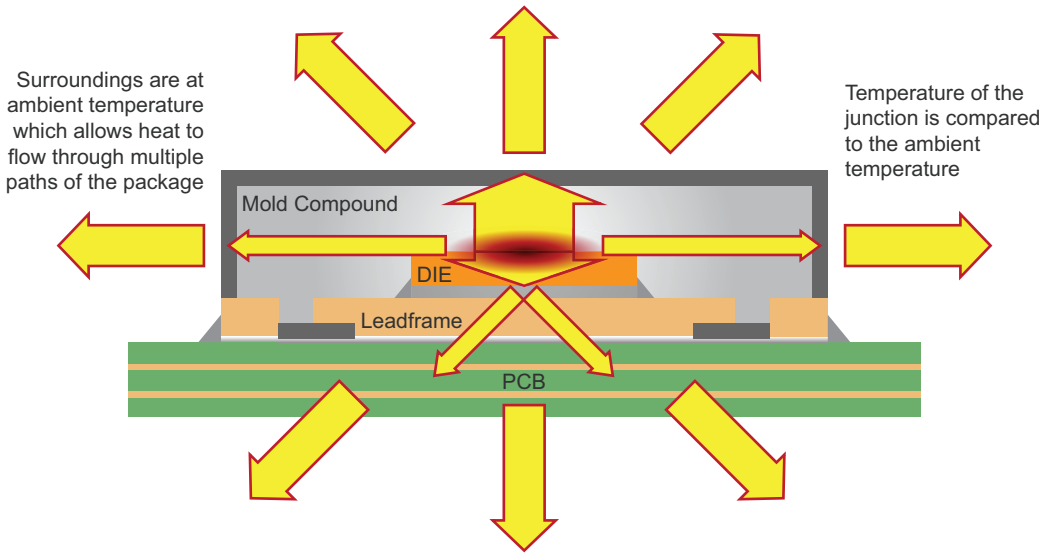
$$T_J = (\Psi_J)(P_{DISS}) + T_X$$

where

X = T (top) or B (board)

Peregrine Semiconductor does not measure Θ_{JT} or Θ_{JB} values. Thermal characterization parameter values, Ψ_{JT} and Ψ_{JB}, are measured and reported. Junction ambient (Θ_{JA}) is also reported as it does not require the use of a heatsink (see **Figure 3**).

Figure 3 ▪ Example of Θ_{JA} Measurement(*)



Note: * Cross-sectional representation of device mounted to printed circuit board (pink arrows represent heat flow).

Determining Thermal Characteristics of Peregrine Packages

Physical testing of Peregrine packages has been established through several different techniques. Thermal imaging of active devices has been used to establish thermal performance for some products. While this technique is not an industry specified method, it has been used to provide an acceptable estimate of the device performance. Peregrine is no longer using this technique for characterization.

The physical measurement of the Θ_{JA}, Ψ_{JT} and Ψ_{JB} values for selected packages is accomplished by following the JEDEC JESD51-2A standard “Integrated Circuits Thermal Test Method Environmental Conditions – Natural Convection (Still Air).” Testing typically makes use of thermal test chips in lieu of active devices for both sapphire and silicon substrates. A variety of die size and package sizes established a matrix of expected values for various combinations of die and package.

Computer simulation is also performed to estimate the performance of a given product under typical or worst case conditions. 3D models are initially created using Solidworks which are then submitted to finite element modeling using ANSYS mechanical software programs. Results have been found to conform well with physical measurements.

Circuit Layout For Thermal Performance

Care must be taken in the development of the layout of the PCB to ensure that all components have adequate thermal dissipation capability. This can be established through proper development of the PCB. Location of components can be a critical factor in controlling the mutual heating and heat dissipation of individual devices. Hotter components must be placed so as to minimize the thermal dissipation onto other components. In addition to component placement, adequate cooling by airflow or heat-sinking is a critical factor for consideration.

The use of the Ψ_{JT} and Ψ_{JB} parameters, along with the Θ_{JA} thermal resistance will allow the designer to more accurately estimate the junction temperature and heat dissipation of the Peregrine component relative to the overall assembly.

Glossary

Θ_{JC} = thermal resistance junction (case)

Θ_{JA}= thermal resistance junction (ambient)

Ψ_{JT} = thermal parameter junction (top)

Ψ_{JB} = thermal parameter junction (board)

P = power

T = temperature

Sales Contact

For additional information, contact Sales at sales@psemi.com.

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