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DTC Theory of Operation

Introduction

The Digitally Tunable Capacitor (DTC) is a variable capacitor controlled by a digital interface. A digital serial interface is used to control CMOS FETs that connect and disconnect fixed High-Q MIM Capacitors to obtain different capacitance values. The use of FET stacking to create a virtual high-voltage FET enables the high power handling of the DTC. The digital control interface is fully integrated on die; no external components for bias voltage generation or interfacing are required. This App Note describes the operation of the DTC and its use in a tunable matching network.

DTC Equivalent Circuit Model

The capacitance of the DTC is determined by the parallel combination of all "on state" MIM capacitor-FET switch paths and all "off state" paths. By weighting each MIM capacitor in the device, a linear and monotonic tuning response is achieved. At the lowest capacitance setting of the device, each switch is off. Figure 1 shows a simplified view of the RF core of the DTC. Figure 2 is the block diagram for the DTC component highlighting the digital interface and RF sections.

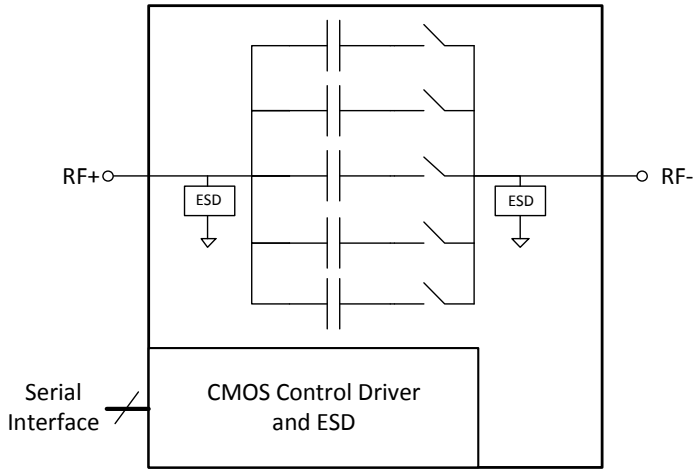

Figure 1: Block Diagram of DTC

Summary

- DTC is a variable capacitor controlled by a digital serial interface
- DTC equivalent circuit model includes 3 main components: Tuning Core, parasitic package inductance, and shunt parasitic network
- Total capacitance in shunt configuration will be higher than series configuration due to parasitic capacitance
- Quality factor is only defined in shunt configuration Peak voltage across the RF terminals or from any RF terminal to ground should not exceed the maximum peak voltage

The DTC can be modeled using a circuit shown in Figure 2. It includes all of the parasitic elements and is accurate in both Series and Shunt configurations. The model reflects physical circuit behavior accurately and provides very close correlation to measured data. The model will match all important parameters (C, tuning range, SRF and Q, mismatch and dissipative loss) properly.

Figure 2 shows the equivalent circuit for the DTC. It includes 3 main components: the Tuning Core composed of R_s and C_s, parasitic package inductance L_s, and the shunt parasitic network (C_p, R_{p1}, R_{p2}).

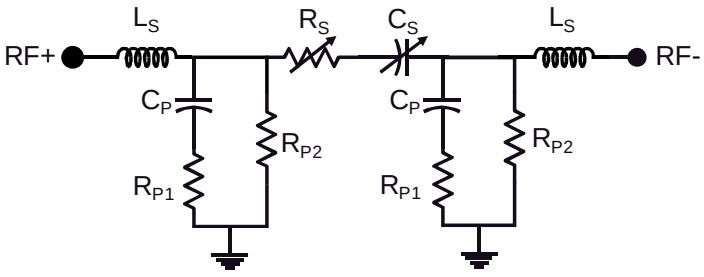

Figure 2: DTC Model

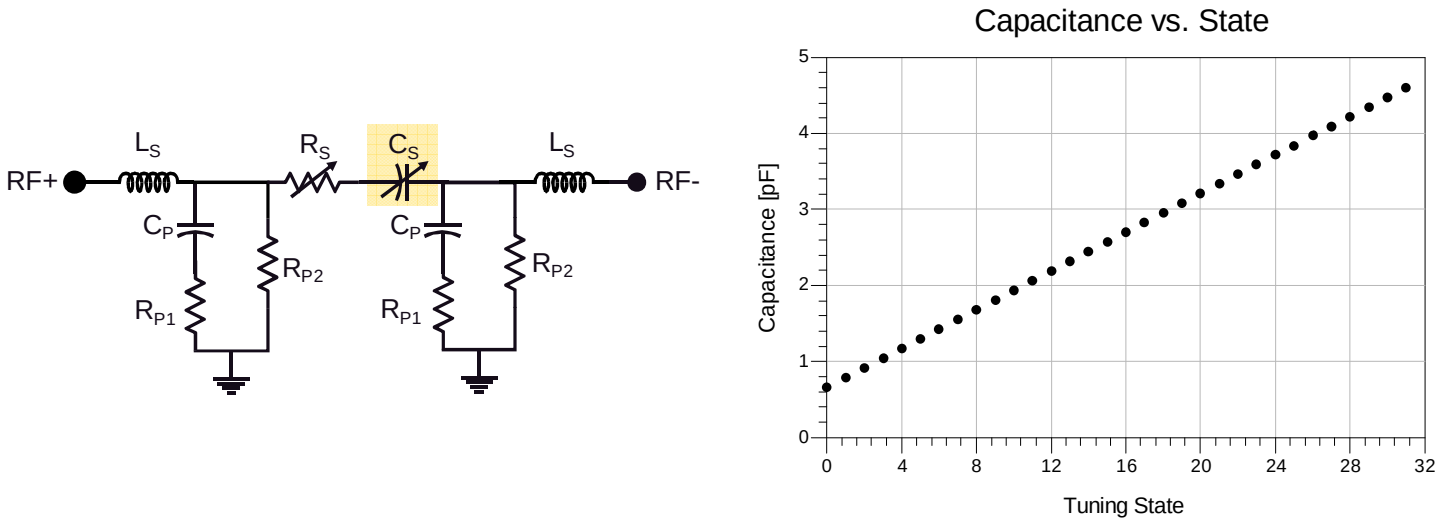

Figure 3: Capacitance of the Tuning Core in Series Configuration

As seen in Figure 3, the Tuning Core capacitance is linearly proportional to the tuning state in a discrete fashion. The Tuning State corresponds to a specific capacitance value that the Tuning Core is programmed to through the serial interface. The resolution of the DTC is determined by the number of capacitance steps that exist between the minimum (C_{smin}) and maximum (C_{smax}) capacitance values. The capacitance tuning ratio of the Tuning Core is determined as $C_{smax}/C_{smin,}$ which is also referred to as the Series Tuning Ratio.

To adequately represent the behavior of a practical implementation of the DTC, the parasitic capacitance (due to circuit and package parasitics) from RF ports to GND (C_p) must be taken into account. Thus the DTC appears as a 3-terminal network and has capacitance between each RF port, and between each RF port to GND. The effective capacitance the DTC presents to a circuit will depend on its configuration (Series vs. Shunt).

In Series configuration, the DTC Tuning Core capacitance C_s is seen between RF+ and RF- ports. In this case, C_s is referred to as the Series Capacitance. Since the shunt parasitic C_p is connected to GND, it doesn't impact the capacitance between RF+ and RF-, but nonetheless must be taken into account when designing the end application circuit.

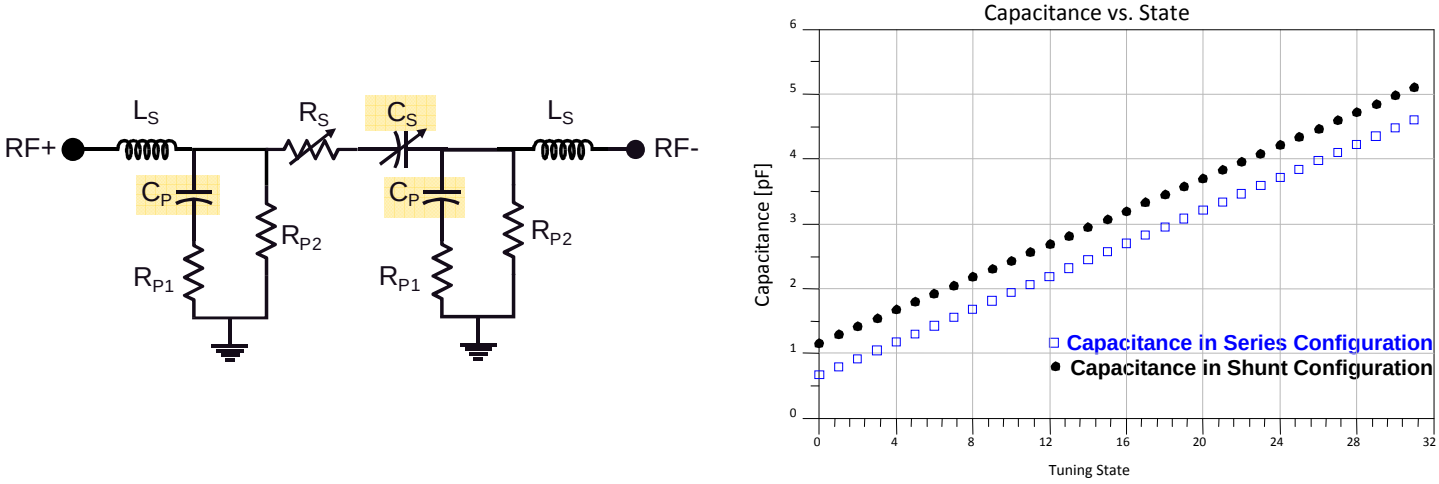

Figure 4: Capacitance in Shunt and Series

In Shunt configuration, typically RF- is grounded and RF+ is connected to the signal. The Package Inductance Ls at RF- port effectively shorts out the parasitic shunt network on the RF- side of the circuit; C_p and Cs become parallel. Thus in shunt, the total capacitance C = (C_s+C_p) is higher than capacitance seen between RF+ and RF- ports, as illustrated in Figure 4.

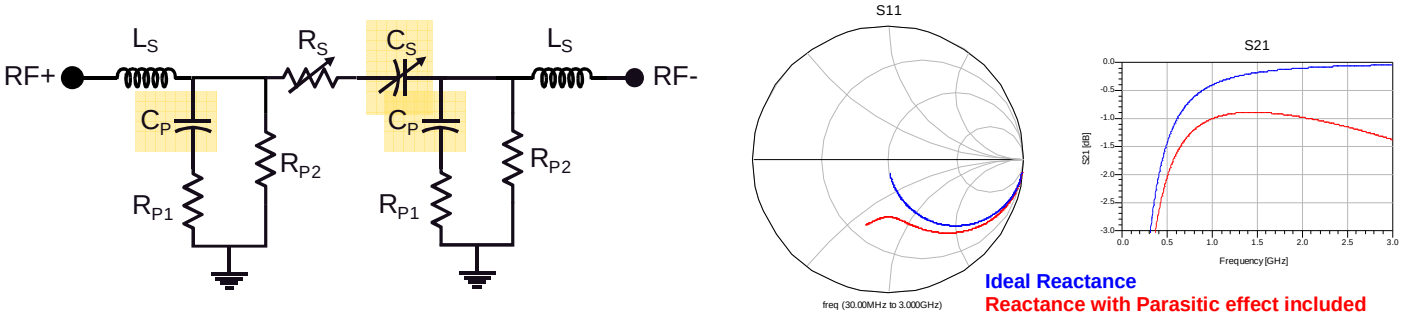

Figure 5: Effect of Parasitic Capacitance on Series Behavior

Since C_p represents shunt admittance, the DTC no longer appears as a simple reactance in series between the RF ports, but rather as an impedance transformer. Thus the S_{11} and S_{21} for the actual circuit in the series configuration deviate from an ideal series reactance, as illustrated in Figure 5.

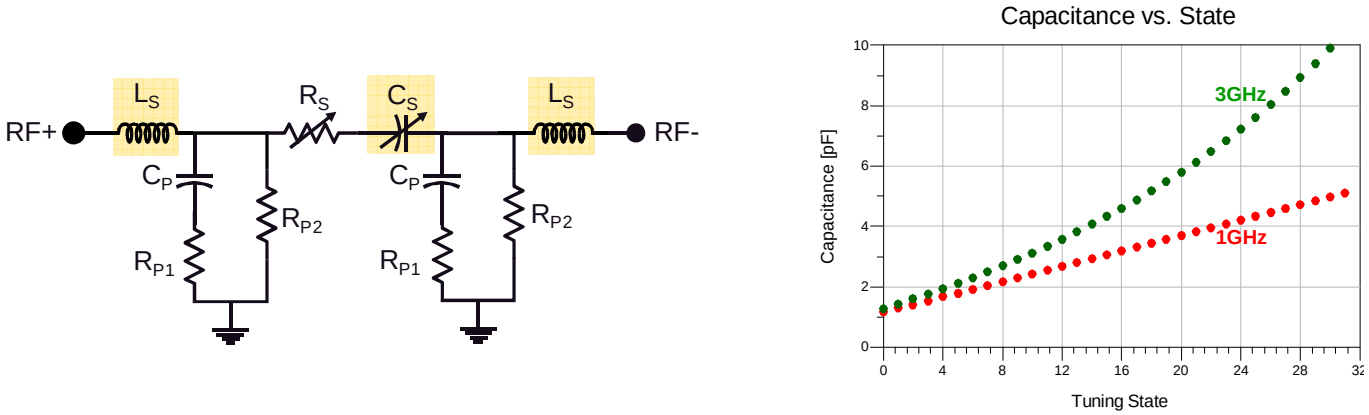

Figure 6: Apparent Capacitance in Shunt Configuration

In addition to the parasitic capacitances, a parasitic inductance L_s (due to package and circuit parasitics) is present in the DTC. This inductance causes the apparent capacitance of the DTC to increase towards higher frequencies. This causes the apparent tuning ratio to also increase at higher frequencies as shown in Figure 6.

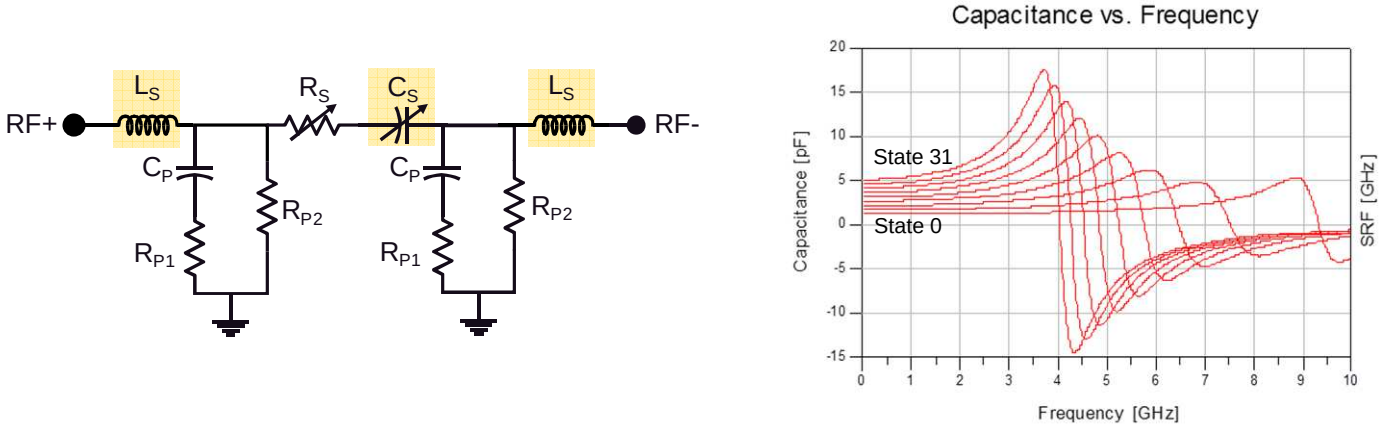

Figure 7: Effects on SRF From Parasitic Inductance

At the Self Resonant Frequency (SRF) the parasitic inductance cancels out the capacitive reactance and capacitance falls to zero. Above SRF the DTC appears inductive (or has negative capacitance).
The SRF is dependent on which tuning state (which capacitance value) the DTC is programmed. SRF is approximately inversely proportional to the square root of capacitance.

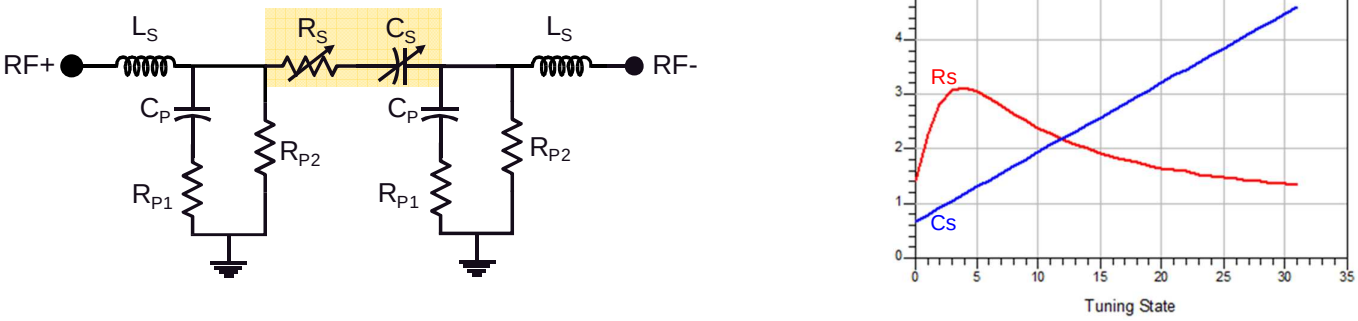

Figure 8: C_s and R_s Dependency on Tuning State

In order to accurately represent the dissipative losses in the DTC, each capacitive element (parasitic or tuning core) must have a resistive component associated with it. The dissipative losses for the Tuning Core (C_s) are modeled by Equivalent Series Resistance (R_s). The value of R_s and C_s depend on tuning state as illustrated in Figure 8.

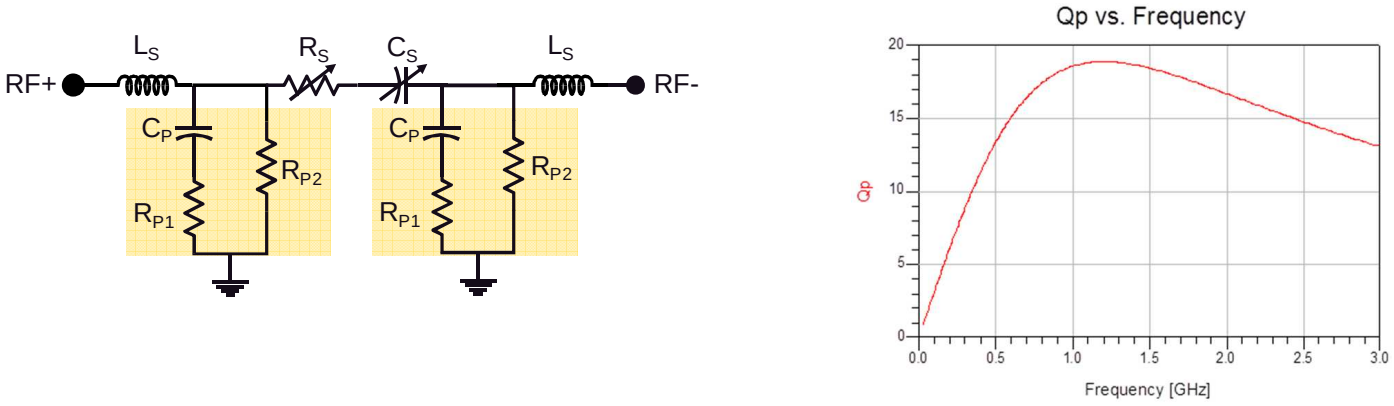

Figure 9: Quality Factor of the Shunt Parasitic Components

The shunt parasitic network is a combination of circuit and package parasitics, which also contain resistive loss components. One source of these resistive losses is the internal biasing circuitry within the tuning core. The component values of the parasitic network are independent of frequency and tuning state. The Quality Factor of the parasitic network (which helps describe its loss) is illustrated in Figure 9.

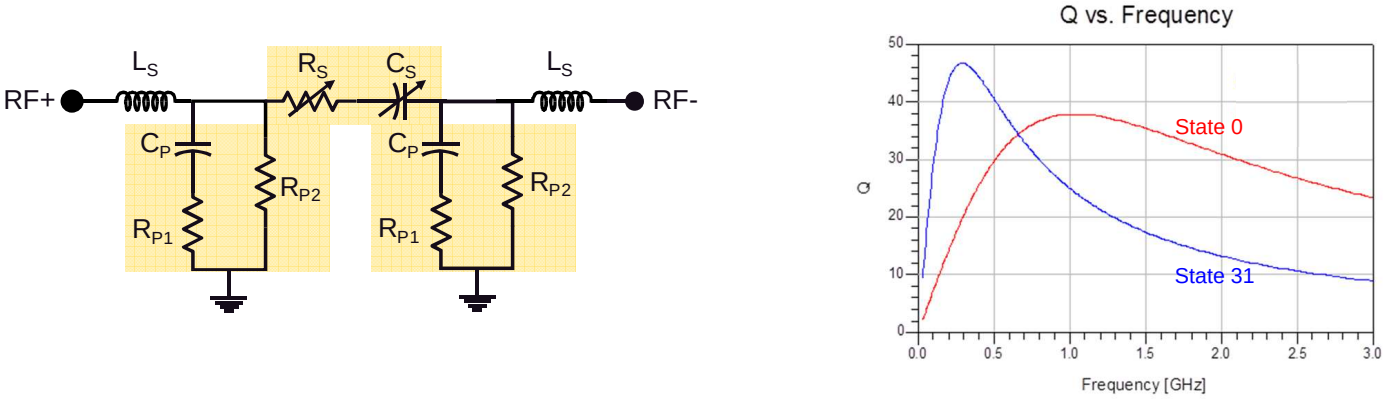

Figure 10: Q as a Composite of Core and Parasitic Components

The complete DTC model provides an accurate representation of the device in both Series and Shunt configurations.

The overall dissipative losses for the DTC depend on the configuration of the part. Quality Factor cannot be defined in general for the DTC connected in Series, because the dissipative losses depend on the source and load impedances. In Shunt configuration however, the RF- is grounded and signal is connected to RF+ port. The total Quality Factor Q in Shunt configuration as seen at RF+ is a composite of the DTC Tuning Core Q_s and the parasitic network components (Q_p), as illustrated in Figure 10.

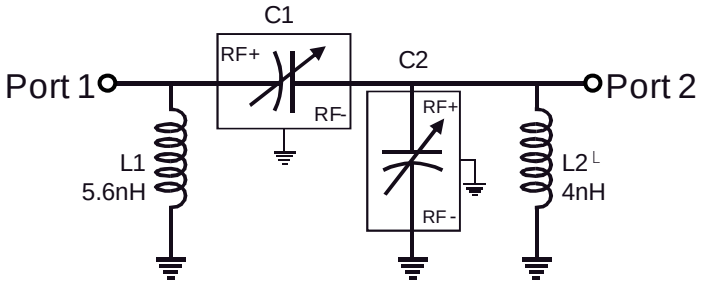

Figure 11: Example Tunable Matching Network

Tunable Matching Network Example

The implementation of an actual Tunable Matching Network using the DTC model is illustrated in Figure 11. Both Series and Shunt DTCs are used to obtain the widest impedance coverage. Shunt inductors are used with the DTCs as part of the impedance transformation network, and to provide the required DC path to ground for proper biasing and additional ESD protection. Their values can be modified to change the frequency response and impedance transformation characteristics of the Tunable Matching Network.

The output impedance constellation of the Tunable Matching Network is shown in Figure 12. Each point on the Smith Chart corresponds to an output load impedance (connected to Port 2) that can be matched to 50 Ω at Port 1 swept over each DTC capacitance state. The Smith Chart constellation is shown for the tuning response present at 1 GHz.

The Insertion Loss and Return Loss plots correspond to selecting tuning states for both DTCs to provide an optimum Return Loss for each frequency point, between 50 Ω ports. Figure 12 shows that the Tunable Matching Network has a bandwidth of 0.75-1.2 GHz, corresponding to a frequency range that can be matched perfectly to 50 Ω. The simulated Insertion Loss of this network is approximately 0.5 dB and accurately represents how the circuit performs in measurement.

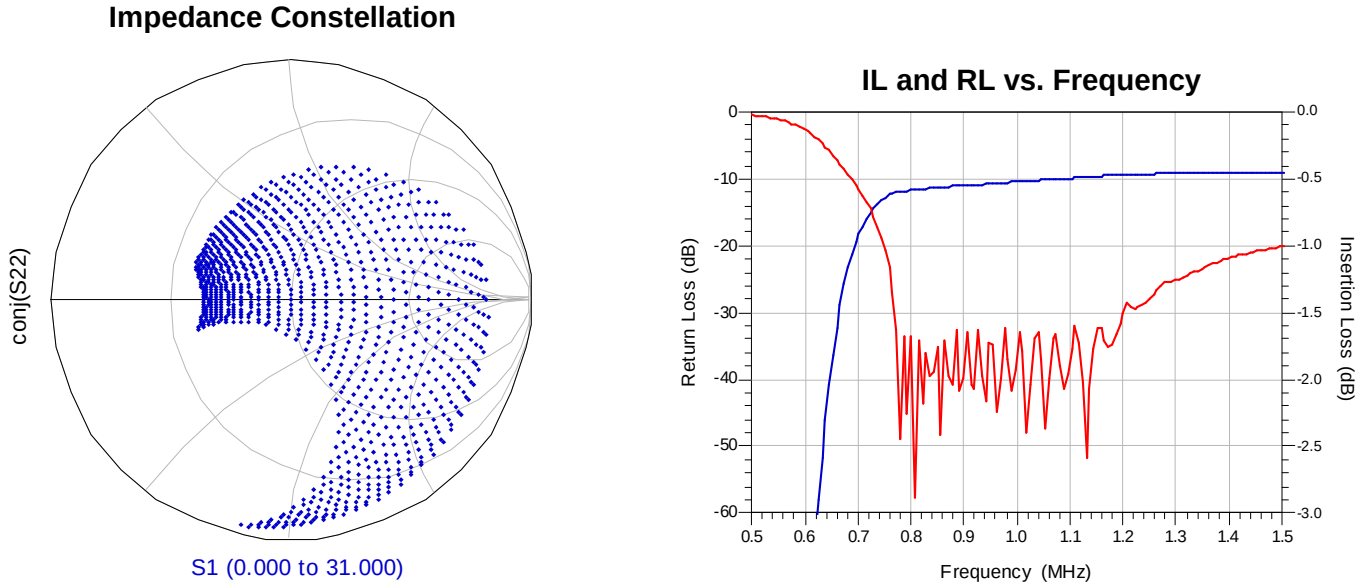

Figure 12: Impedance Matching Network Response

Design Guidelines (Peak RF Voltage limit)

Reconfigurable circuits such as filters and matching networks often expose components to high peak voltages because of the transformation ratios seen in the resonating elements in the circuit. The RF voltage across the DTC is dependent on the impedance and RF power level. In some circuits such as filters or impedance matching networks, certain source and load impedances can cause the effective RF voltage across the DTC to exceed maximum specified V_{pk} even at low RF input power.

Since the DTC contains ESD protection circuitry, a path to ground exists at each RF terminal even if it is used in a series configuration. In addition to the RF voltage present across the RF terminals of the device, care must be taken not to exceed maximum specified V_{pk} between any RF terminal and ground (RF+ to Ground or RF- to Ground). Spurious emissions will increase if the V_{pk} limit is exceeded between the RF+ and RF- terminals and between the RF+ terminals and ground.

To demonstrate this, the example tuner presented earlier is evaluated with a 34 dBm 1 GHz input (50 Ω) at Port 1 and a load impedance (Z_L) swept over all phase angles for VSWR values of 1:1, 3:1, and 9:1 at Port 2. In this case, a DTC with 30 V_{pk} voltage handling is assumed.

The effective peak voltage across the DTC can be solved mathematically, typically by use of simulation software such as ADS or MATLAB. In the example shown in Figure 13, the source impedance (Port 1) is set to 50 Ω while the load impedance (Port 2) is swept over VSWR and phase to cover various impedance conditions. At each VSWR and phase, the capacitance values for DTCs A and B are chosen to achieve the lowest mismatch loss between Ports 1 and 2. With this, the peak voltage each DTC will be exposed to can be solved.

Figure 14 shows the solved peak RF voltages across the various terminals of DTCs A and B over various load impedances. As can be seen, over all load impedances of up to 9:1 VSWR, 30 V peak RF is never reached for DTC A between the RF+ terminals to ground, or between the RF+ and RF- terminals.

Unfortunately, with this design, some load impedances presented at Port 2 cause 30 V to be exceeded across the RF+ and RF- (ground) terminals of DTC B. Because of this, this design shouldn't be used at some load impedances at 9:1 with 34 dBm input power, or the input power must be reduced.

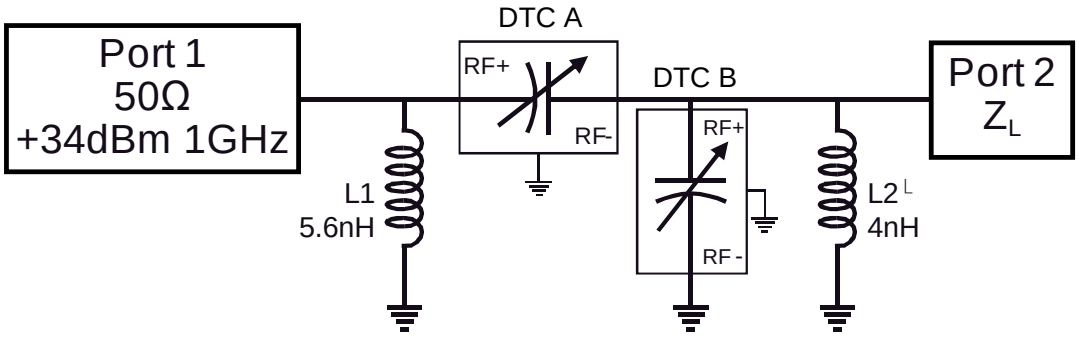

Figure 13: RF Voltage Example

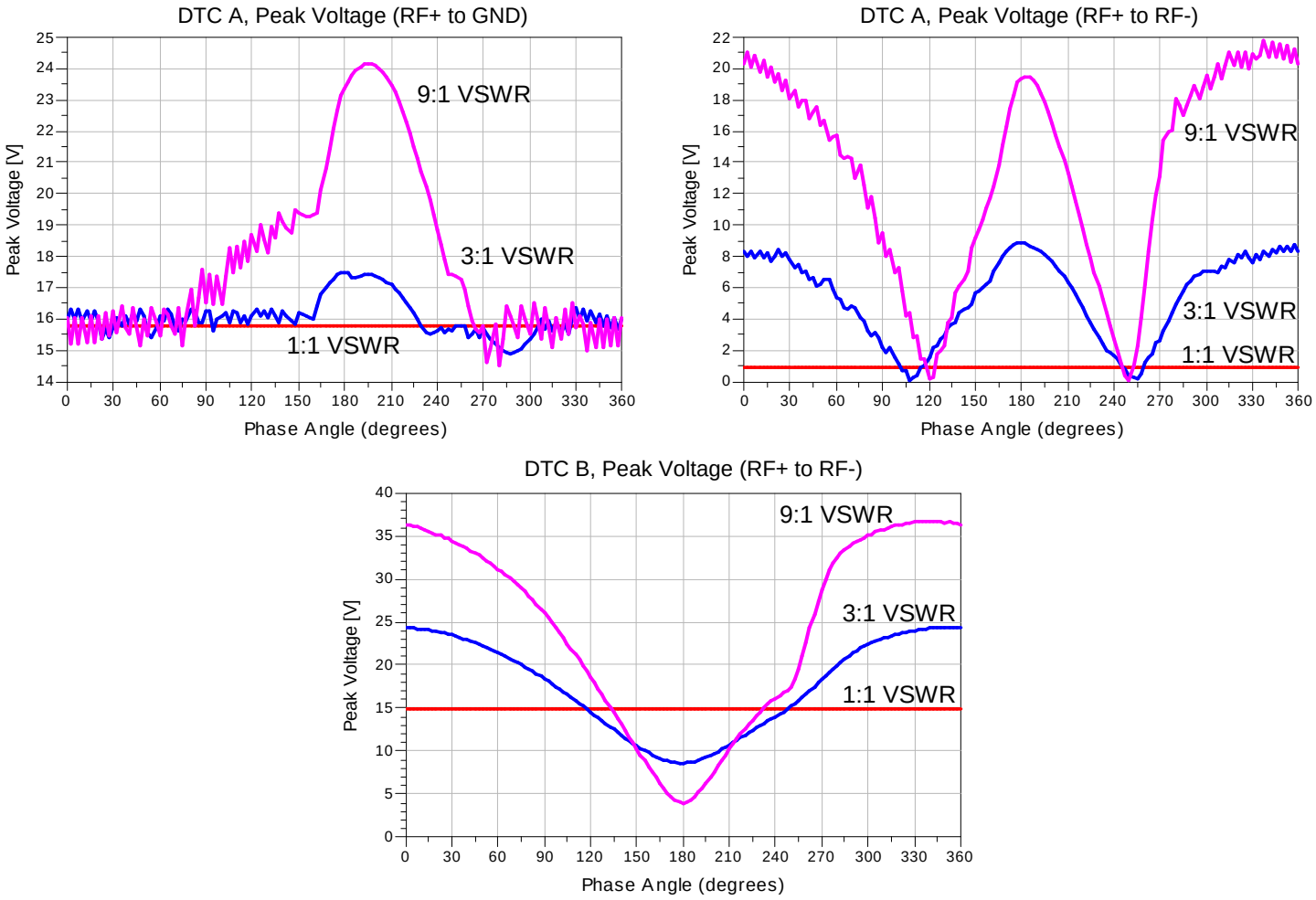

Figure 14: RF Voltages for Example Tuner with 34 dBm Input

Conclusion

The DTC theory of operation has been described. The DTC is variable capacitor controlled by a serial interface that is integrated on die with the Tuning Core. Applicable to both series and shunt configurations, the DTC can be modeled with three main sections - a Tuning Core, a parasitic inductance, and a shunt parasitic network. The parasitic elements affect the total capacitance in shunt and the apparent capacitance at higher frequencies. The overall dissipative losses of the DTC, described as the Quality Factor, are defined only in shunt configuration. If the DTC is used in filters or impedance matching networks, care must be taken not to exceed the maximum specified peak voltage between RF terminals or from any terminal to ground.