

Advantages of UltraCMOS™ DSAs with Serial-Addressability

Introduction

Today's RF systems are more complex than ever as designers seek to integrate more functionality into their products. Achieving this functionality requires reliably controlling many ICs.

For years, high-performance RF and microwave products have relied heavily on GaAs technology. While GaAs provides good RF performance, it has a few limitations. Digital circuitry requires a lot of power and is not easy to implement. Control is usually limited to simple parallel and serial methods, often executed with costly, complex, and less reliable multi-chip modules (MCM).

On the other hand, UltraCMOS™ technology is much more versatile than GaAs technology. Peregrine's UltraCMOS Digital Step Attenuators (DSAs) provide best-in-class linearity and attenuation accuracy, and fast settling time. Also, digital and RF functions are easily integrated, enabling superior control methods without resorting to MCMs.

Many RF designers may be unfamiliar with serial-addressable control. This application note describes the basic operation of parallel, serial, and serial-addressable control and the advantages of UltraCMOS DSAs with serial-addressability.

Summary:

This Application Note provides an overview of Parallel, Serial, and Serial-Addressable control in UltraCMOS™ DSAs.

A unique feature of UltraCMOS DSAs, Serial-Addressable control has the following advantages:

- Control up to eight devices with only three communication lines
- Simplified and more compact layouts
- Better noise immunity
- Control of multiple devices with little additional complexity

Peregrine's DSA product offerings provide the designer with flexibility to meet varying system needs. See page 7 for a comparison table of UltraCMOS DSAs.

Parallel Control

Parallel control is commonly available on both GaAs DSAs and UltraCMOS DSAs. In direct-parallel control, the microcontroller unit (MCU) programs the logic level on each control pin directly to the desired attenuation level. In latched-parallel control, the MCU first programs the logic levels into a temporary register which is then latched into the control pins by pulsing Latch Enable (LE) from high to low. Direct-parallel and latched-parallel control are illustrated in Figures 1 and 2.

In both cases the MCU commands Peregrine's **PE43702**, a high-linearity, 7-bit DSA that covers a 31.75 dB attenuation range in 0.25 dB steps. The DSA provides a direct-parallel, latched-parallel, or serial CMOS control interface. In direct-parallel control the MCU sends data from its parallel outputs (PO#s) to the DSA's control inputs (C#s). Logic high activates an attenuation setting and logic low deactivates an attenuation setting. For example, for maximum attenuation, the MCU sends logic high to all control inputs. For minimum attenuation, the MCU sends logic low to all control inputs. For all other attenuation levels, the MCU sends logics high and low in the appropriate combination. The only difference for latched-parallel control is that the control commands are stored in a temporary register and latched simultaneously with the LE line.

Parallel control has the advantage of speed compared to serial control. The disadvantage is the use of multiple control lines, which require much more board space and a more complicated layout to isolate the RF subsystem from the control lines and other noise sources. This disadvantage is compounded in designs requiring multiple DSAs.

Figure 1. Direct-Parallel Control

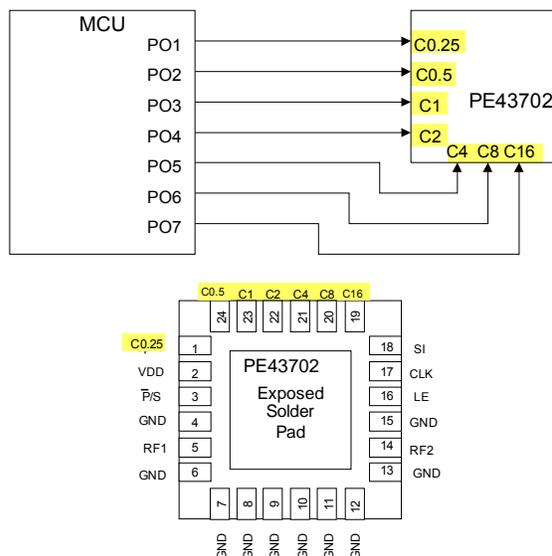
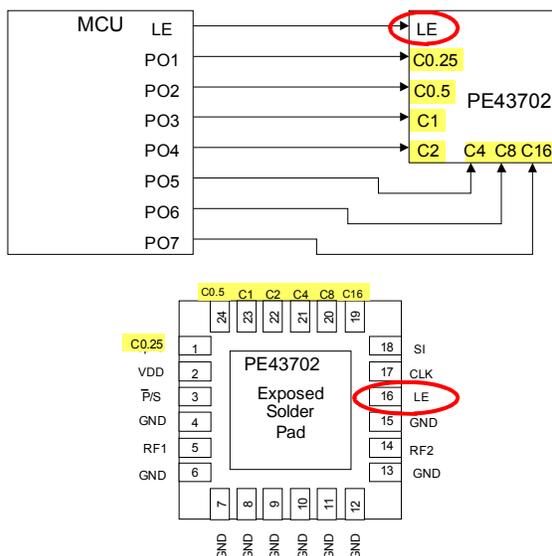


Figure 2. Latched-Parallel Control

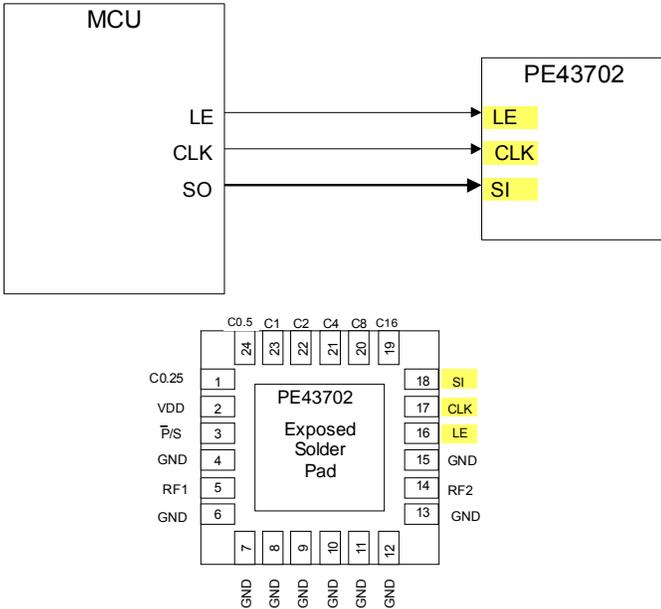


Parallel programming (Figures 1 and 2): The desired attenuation level is programmed directly onto each control pin (direct-parallel) or indirectly latched onto each control pin (latched-parallel).

Serial Control

Now consider PE43702 configured for serial control, illustrated in Figure 3. Serial control is also commonly available on both GaAs and UltraCMOS DSAs.

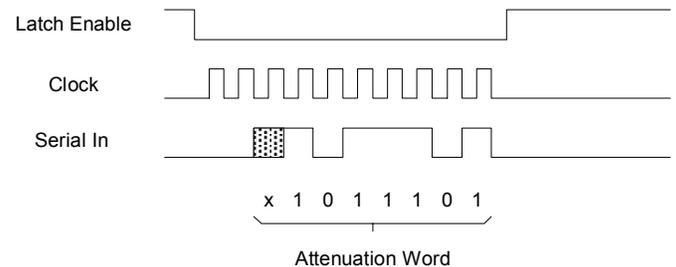
Figure 3. Serial Control



Consider an example where PE43702 is to be serially programmed to 23.25 dB of attenuation. Since PE43702 has 0.25 dB steps, the remaining bits may be calculated by multiplying the desired level by four and converting to binary, remembering to include the “don’t care” for the most significant bit: $23.25 \times 4 = 93 \rightarrow (X1011101)_2$.

Figure 4 shows the resultant timing diagram of the three inputs of PE43702. First LE is changed to logic low. Next, the MCU initiates the CLK signal. Then the MCU sends the Attenuation Word to SI, clocking in each word bit. LE is returned to logic high after the eighth word bit is clocked in, latching the Attenuation Word into the DSA and setting the attenuation to 23.25 dB. Note that new data cannot be written to the SI register until any previous data transfer is complete and LE is reset to logic low.

Figure 4. Example Timing Diagram, Serial Control



Serial programming: Attenuation is programmed within a one-byte Attenuation Word, least significant bit first.

Serial control is implemented using a master/slave relationship. The MCU is the master device and initiates communication by changing LE from logic high to logic low. The MCU then generates a clock (CLK). Data may now be transferred from the MCU’s Serial Out (SO). Attenuation is programmed with a one-byte (i.e., eight bit) Attenuation Word. Since PE43702 requires only seven bits, the Attenuation Word’s most significant bit is a “don’t care.” Data bits are shifted into Serial In (SI) on the rising edge of CLK, least significant bit first. SI is a line of shift registers that stores each bit until the latch is enabled.

The main advantage of serial control is reduced routing complexity. For PE43702, control lines have been reduced from seven in direct-parallel mode to three in serial mode. Isolation considerations are therefore also simplified. The main disadvantage of serial control is slower speed; however, clock speeds in modern electronic systems are so fast that this is often not a problem.

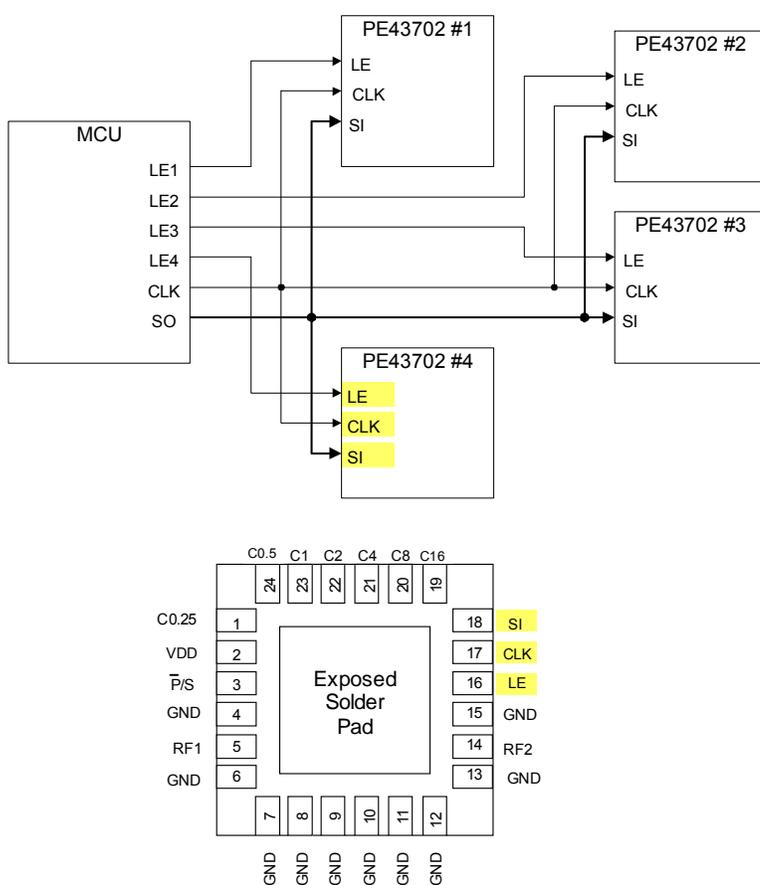
Serial control is relatively easy to adapt to controlling multiple devices, as illustrated in the example in Figure 5.

This implementation has one master device and four slave devices. Each PE43702 is configured for serial control, and each has its own LE line from the MCU. To program, for example, 23.25 dB of attenuation to only PE43702 #2, set LE1,

LE3, and LE4 to a logic high and cycle LE2, latching in the appropriate Attenuation Word $(X1011101)_2$.

Unfortunately, the effect is that the parallel lines that serial control helped eliminate in the single device case are added back in, and the same problems recur - larger, more complicated layouts and reduced RF isolation.

Figure 5. Serial Control of Multiple Devices

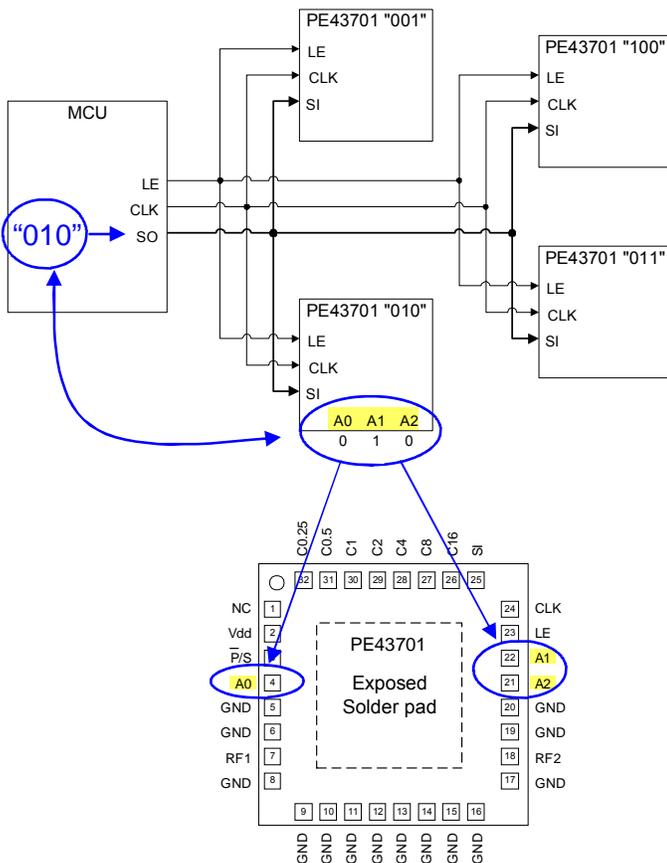


Serial programming of multiple devices:
Attenuation is programmed by setting the appropriate LE level to each device.

Serial-Addressable Control

The real benefits of serial-addressable control may now be seen, as illustrated in Figure 6. Serial-addressable control is a unique feature of UltraCMOS DSAs that is not available in GaAs DSAs. Table 1 (see page 7) details the programming options of Peregrine’s DSAs.

Figure 6. Serial-Addressable Control



In this example, the MCU commands the **PE43701**, a high-linearity, 7-bit DSA that covers a 31.75 dB attenuation range in 0.25 dB steps. The DSA provides a direct-parallel, latched-parallel, and serial-addressable CMOS control interface. The DSAs are also identified by hard-wiring address pins A2, A1, and A0 on the PE43701 package.

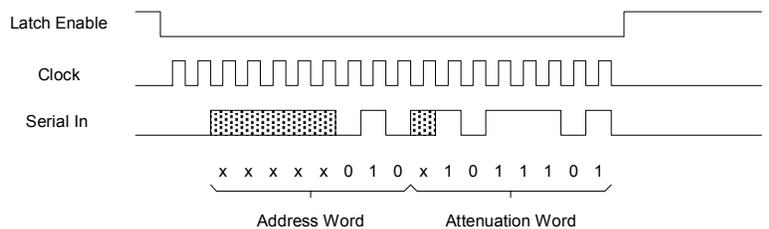
Where serial mode used one-byte protocol, serial-addressable mode uses two-byte protocol. The most significant byte (MSB) is the *Address Word* and the least significant byte (LSB) is the *Attenuation Word*. The three least significant bits of the Address Word are address bits (bit 2 for A2, bit 1 for A1, and bit 0 for A0), allowing up to eight addresses for programming.

Like PE43702, the seven least significant bits of PE43701’s Attenuation Word program its attenuation level. Unused bits in either word are “don’t cares”. Figure 7 shows the timing diagram of the three inputs of PE43701 “010” to program 23.25 dB attenuation in serial-addressable mode.

The Address Word identifies device “010” in its three least significant bits. The Attenuation Word is derived using the same method as serial control with a single device, so once again use $(X1011101)_2$. Although all four DSAs see the same LE, CLK, and SI, only DSA “010” will be programmed.

Serial-Addressable programming: Only the DSA whose physical address (set on the DSA package pins) matches the Address Word will be programmed. All other DSA’s will ignore the programming command.

Figure 7. Example Timing Diagram for Serial-Addressable Control

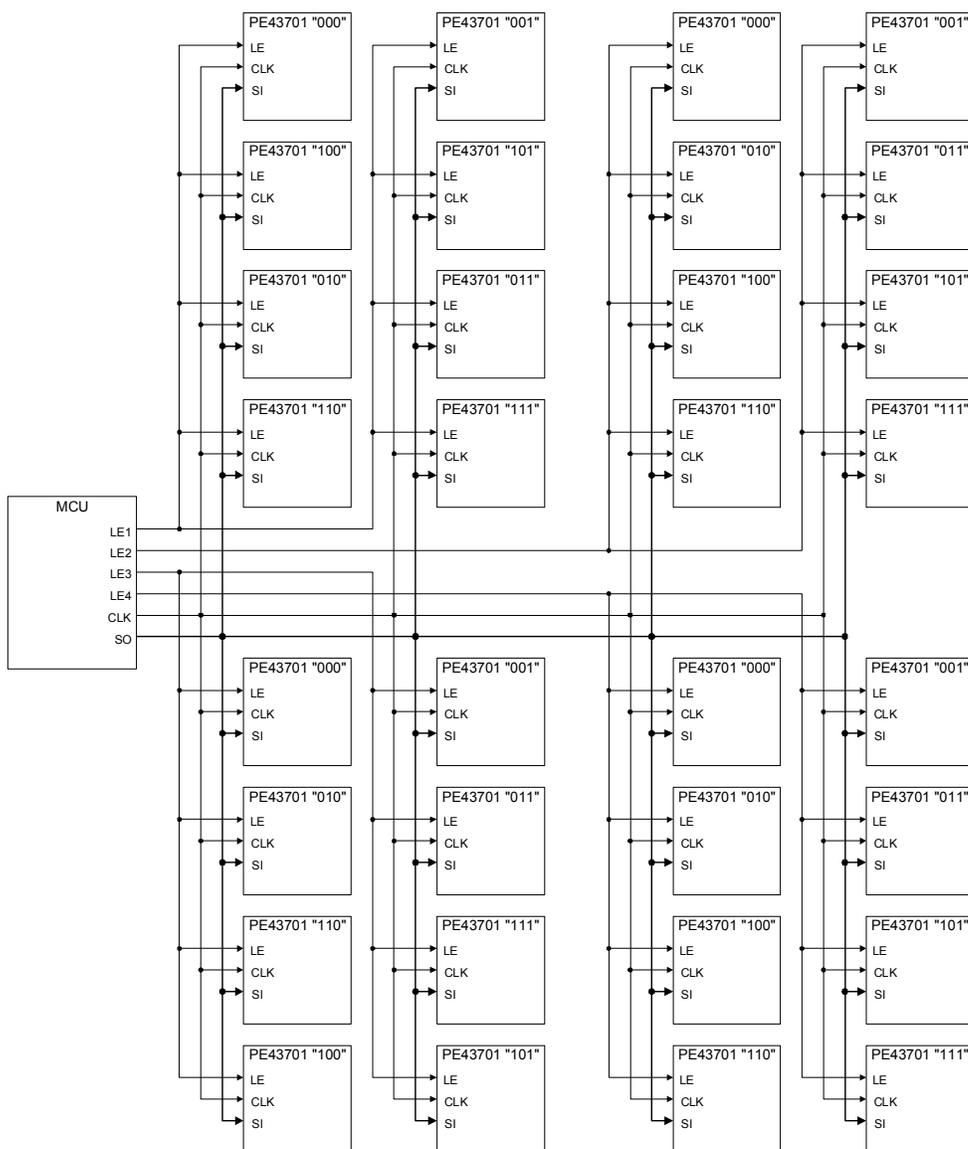


Serial addressability in Peregrine's DSAs extends the advantages of simple serial control of one device to the control of many more – only three lines are required for up to eight devices, reducing board size and simplifying design. Adding latch lines also makes it relatively easy to control 16, 24, or even more DSAs, as illustrated in Figure 8. In this example, six communication lines control 32 devices with serial-addressability, a more

practical implementation than using thirty-four communication lines to control 32 devices without serial-addressability. In general, for x devices without serial addressability 2 + x communications lines are required; with serial addressability, only 2 + INT[(x + 7) / 8] lines are required.

Note: Buffering may be required for CLK and SO to drive 32 devices.

Figure 8. Serial Addressable Control of 32 devices



Serial-Addressable Programming of multiple devices: an MCU with multiple LE lines extends the advantages of Serial-Addressable control. Note: Buffering may be required for CLK and SO to drive 32 devices.

Conclusion

UltraCMOS™ DSAs offer many advantages over GaAs DSAs, and serial-addressability is a particularly valuable advantage. Parallel control of DSAs provides fast attenuation programming but requires a great amount of board space and compromises noise immunity. Serial control, on the other hand, offers simpler layouts and better noise immunity, especially for controlling a few ICs. Serial-addressable control, a unique feature of Peregrine DSAs, extends the advantages of serial control of one device to many more,

empowering the designers of today's increasingly sophisticated RF products.

For help or more information about this Application Note, please contact Peregrine Applications Support at help@psemi.com.

Datasheets can be found on our website at www.psemi.com.

Table 1. Comparison of UltraCMOS DSAs

Part #	Product Description	Freq. range (GHz)	Attenuation (dB)	Insertion Loss (dB)	Input IP3 (dBm)	Package	Programming Modes			
							Direct Parallel	Latched Parallel	Serial	Serial-Addressable
PE43404	4-bit, 75 Ω	DC-2.0	15 range 1.0 steps	1.4	52	20-lead 4x4 QFN	yes	yes	yes	no
PE4305	5-bit, 50 Ω	DC-4.0	15.5 range 0.5 steps	1.5	52	20-lead 4x4 QFN	yes	yes	yes	no
PE4306	5-bit, 50 Ω	DC-4.0	31 range 1.0 steps	1.5	52	20-lead 4x4 QFN	yes	yes	yes	no
PE4307	5-bit, 75 Ω	DC-2.0	15.5 range 0.5 steps	1.4	52	20-lead 4x4 QFN	yes	yes	yes	no
PE4308	5-bit, 75 Ω	DC-2.0	31 range 1.0 steps	1.4	52	20-lead 4x4 QFN	yes	yes	yes	no
PE4302	6-bit, 50 Ω	DC-4.0	31.5 range 0.5 steps	1.5	52	20-lead 4x4 QFN	yes	yes	yes	no
PE4309	6-bit, 50 Ω	DC-4.0	31.5 range 0.5 steps	1.6	52	24-lead 4x4 QFN	yes	yes	no	no
PE4304	6-bit, 75 Ω	DC-2.0	31.5 range 0.5 steps	1.4	52	20-lead 4x4 QFN	yes	yes	yes	no
PE43701	7-bit, 50 Ω	DC-3.0	31.75 range 0.25 steps	1.6	57	32-lead 5x5 QFN	yes	yes	no	yes
PE43702	7-bit, 50 Ω	DC-4.0	31.75 range 0.25 steps	1.7	57	24-lead 4x4 QFN	yes	yes	yes	no
PE43703	7-bit, 50 Ω	DC-6.0	31.75 range 0.25, 0.5 or 1.0 steps	1.6	57	32-lead 5x5 QFN	yes	yes	no	yes

The information in this document is believed to be reliable. However, Peregrine assumes no liability for the use of this information. Use shall be entirely at the user's own risk.

No patent rights or licenses to any circuits described in this document are implied or granted to any third party.

Peregrine's products are not designed or intended for use in devices or systems intended for surgical implant, or in other applications intended to support or sustain life, or in any application in which the failure of the Peregrine product could create a situation in which personal injury or death might occur. Peregrine assumes no liability for damages, including consequential or incidental damages, arising out of the use of its products in such applications.

The Peregrine name, logo, and UTSi are registered trademarks and UltraCMOS, HaRP and MultiSwitch are trademarks of Peregrine Semiconductor Corp.